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The influences of surface states on the metal - oxide - semiconductor high frequency c - v curves

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THE INFLUENCES OF SURFACE STATES ON THE METAL - OXIDE - SEMICONDUCTOR HIGH FREQUENCY C - V CURVES

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The effects of surface states located in the Si-SiO_2 interface on the high frequency C-V curves were studied theoretically and experimentally.

The theory of dynamic charge current and capacitance characteristics in MOS structures with distributed surface states by Simmons and Wei was extended to a more realistic non-uniform surface state distribution approximating the measured state distribution, for convenience, by a three part step form, consisting of a low state density region in silicon mid-gap and two high state density regions near the band edges, the following theoretical results were obtained:

In steady-state, the emission of trapped electrons from surface states reduces the slope of the C-V curve below its ideal value without states. A charging and discharging of the high surface state density near the valence band edge (for N-type) explains the measured capacitance ledge.

In non-steady-state, the emission of trapped electrons is too low to fully respond to the voltage ramp. Therefore, the emission becomes a function of time, and the calculated C-V curve shows deep depletion.

Experimental C-V curves at 1MHz were plotted for three samples, and the corresponding surface state distributions determined employing the high frequency and the quasi-static method. Reasonable agreement was found between the C-V curves plotted with 71mv/sec ramping rate at 300°K and the calculated steady-state curves.

Deep depletion of the experimental C-V curves was observed in

non-steady-state, but, then capacitance saturated with increasing negative voltage ramp contray to the theoretical curve. This discrepancy was explained by generation of minority carriers in the silicon depletion layer that was neglected in the dynamic theory.

One sample showed an increase of the non-steady-state capacitance in deep depletion when the negative slope of the voltage ramp was applied. This effect was explained by mobil negative ions on the outer oxide surface.

1. INTRODUCTION

Silicon has been widely used in electronic device fabrication since the development of the planar process. During fabrication, silicon dioxide layers are grown as protection on the silicon bulk. The interfacial phenomena at Si-SiO_2 interface influence the characteristics of the these devices. For example, the presence of surface states affects the current-voltage characteristics of the insulated gate field effect transistor by altering the channel width and the threshold voltage. Also 1/f noise is caused by surface states. (1)

1.1 Historic Background

The existence of localized electronic states within the forbbidden band gap of semiconductor surface was theoretically predicted by Tamm and Shockley (2) as consequence of non-periodicity of the potential at the surface of the solid. Bardeen (3) postulated interface states at the metal-semiconductor contact. Experiments by Shockley and Pearson (4) proved experimentally the existenceof surface states. Finally, the invention of transistors gave great impetus to intensive studies of semiconductor surface.

Most of the earlier work was concentrated on vacuum cleaved surfaces, but recent research has focused on oxidized silicon surfaces in view of their importance in planar silicon-technique.

Ever since the metal-oxide-semiconductor (MOS) structure was proposed as a voltage dependent capacitor (5,6) and its equivalent

circuit was suggested (7), MOS structures have been frequently employed in the investigation of $Si-SiO_2$ interface properties. Various methods have been introduced to determine the surface state distribution. Of particular importance are the high frequency method introduced by Terman (8), the low frequency method by Berglund (9), the conductance method by Nicollian and Goetzberger (10), the temperature variation method by Gray and Brown (11), and the quasi-static method by Castegne (12) and Kuhn (13). These measurements revealed a continuous distribution of surface states in the band gap with densities from 10^{10} to 10^{13} $ev^{-1}cm^{-2}$.

The capacitance-voltage characteristics of a MOS structure with surface states at the $Si-SiO_2$ interface were extensively investigated by Grove et al (14) explaining the characteristics qualitatively and quantitatively. The frequency dispersion of the MOS capacitance-voltage and conductance voltage characteristics was studied in detail by Nicollian and Goetzberger (10), and a simple equivalent circuit of the device was confirmed.

Measurements of MOS devices at low temperature show some anomalous characteristics. They are interpreted as a combined effect of surface states and externally supplied minority carriers (15-17). The capacitance ledge of the capacitance-voltage curve measured with a positive-slope linear voltage ramp for a N-type (cf. Fig. 4 of ref. 15) was used to estimate the surface state density and the rate of electrons captured by surface states (16). A peak found on a C-V curve for a negative-slope linear voltage ramp was explained by generation of carriers from surface states (17).

The recombination velocity caused by states at the $Si-SiO_2$ interface

was measured by Zerbst (18). In very thin oxide (<100A), electrons and holes can tunnel through the oxide via surface states (19). The corresponding theory of tunneling was developed by Freeman and Dahlke (20), and their model experimentally confirmed by Card and Rhoderick (21).

Recently, Simmons and Wei (22,23) proposed a theory of dynamic charge current- and capacitance-characteristics in MOS structures containing surface states. They used a uniform distribution of surface states in the silicon energy gap to interpret the measured capacitance ledge and the deep depletion at low temperature. However, since such a uniform surface state distribution is unrealistic, a modification of this model is needed and will be presented in this thesis.

1.2 Objective of This Thesis

The objective of this thesis is to investigate experimentally and theoretically the influence of surface states on high frequency C-V curves. Simmons' theory is extended by introducing a more realistic surface state distribution in Chapter 2. The dynamic theory (23) of surface states is applied to an idealized non-uniform distribution of surface states, and theoretical capacitance-voltage characteristics at steady-state and non-steady-state condition are derived.

Experiments on three samples are discussed. Their fabrication is explained in Chapter 3. A detailed procedure of pre-oxidation wafer treatment is listed in Appendix E.

A brief description of two methods for measuring the surface state density used in this thesis is given in Chapter 4. Theory, procedure and merits of each method are presented and discussed.

Chapter 5 contains experimental results and their discussion. High frequency C-V curves (1MHz) for different temperatures are shown. The surface state distributions are approximated by simple step forms. Then C-V curves are calculated extending Simmons' theory and compared with measured curves. Reasonable agreement is noted; small discrepancies are qualitatively explained.

2. THEORY OF DYNAMIC CHARGE CURRENT- AND CAPACITANCE- CHARACTERISTICS IN MOS STRUCTURES

A MOS structure consists of a silicon substrate, a layer of silicon dioxide of thickness X_o and a metal electrode as shown in Fig. 1a. V is the voltage applied to the metal electrode. A MOS structure is called ideal (14), if 1) the work function difference between metal and silicon substrate vanishes, 2) no charges are in the oxide layer, 3) no surface states are at the $Si-SiO_2$ interface and 4) zero bulk resistance is assumed. The oxide capacitance is $C_{ox} = \epsilon_{ox}/X_o$.

Figure 1b shows the band diagram of an ideal MOS structure with N-type silicon substrate. Without applied voltage, thermal equilibrium requires the Fermi level to be constant through the metal and the silicon, and conduction- and valence-band are flat, corresponding to flat band condition. If a negative voltage V is applied (Fig. 1b), the Fermi level of the metal is raised by an amount |V| with respect to the Fermi level of the semiconductor. All charges in the metal , assuming a perfect conductor, reside at the metal-oxide interface. The majority carriers of the semiconductor, i.e., electrons, are repelled, a depletion region of thickness X_d is formed, and the silicon-bands are bent upward.

Figure 2 shows calculated high frequency, low frequency and deep depletion capacitance-voltage curves of an ideal MOS structure with an N-type substrate of 10^{15} cm^{-3} doping. In region a to b of Fig. 2, the silicon is in accumulation with majority carriers accumulated at the $Si-SiO_2$ interface. Point b corresponds to flat band condition. Feature b to c corresponds to depletion or weak inversion. Point c indicates onset of strong inversion, and the capacitance is constant from c to d. Region

b to e shows deep depletion without formation of an inversion layer in silicon.

In practical MOS structures, the C-V curves are additionally influenced by (14,24,25)

1) the work function difference between metal and silicon, $\phi_{ms} = \phi_m - \phi_s$

2) the fixed oxide charge, Q_o; and

3) fast surface states at the Si-SiO2 interface of density N_{ss} ev^{-1} cm^{-2}.

To maintain the MOS structure with applied voltage in thermal equilibrium, the work function difference, ϕ_{ms}, causes a band bending in silicon near the $Si-SiO_2$ interface, and results in a shift of the C-V curve.

A fixed positive oxide charge, Q_o, located in SiO_2 within 200A of the $Si-SiO_2$ interface (26) cannot communicate with the silicon bulk. These states are referred to as slow surface states. Their presence shifts the C-V curves to the left corresponding to a voltage shift $\Delta V = -Q_o/C_{ox}$.

Fast surface states usually result from the non-periodicity of the silicon potential at the surface. Their density on freshly cleaved silicon surfaces is roughly equal to the density of dangling bonds at the surface ($\approx 10^{14}$ cm^{-2}). These unsaturated bonds exhibit a strong attraction for foreign impurities, which become attached to the surface by absorption and chemisorption. When an oxide layer is grown on this silicon surface, a number of these bonds are bound by the oxide resulting in a reduction of the state density to about 10^{10} to 10^{13} cm^{-2} (27). Grove et al (14) found that surface states cause a deviation from the ideal C-V curve.

In this thesis, fast surface states are for convenience called

surface states, and slow surface states referred to as fixed oxide charge.

A theory of dynamic charge current- and capacitance-characteristics in MOS structures has been developed by Simmons and Wei (22,23) that explains the effect of a uniform surface state distribution in the silicon band gap. But, since the state distribution as measured by Nicollian and Goetzberger (10), Gray and Brown (11) is known to be non-uniform (Fig. 3a); a modification of this model is required.

It is therefore proposed to approximate the surface state distribution of Fig. 3a by a three-part step-form shown in Fig. 3b and then, to apply Simmons and Wei's theory. In Fig. 3b, the surface state density is N_{st1} $ev^{-1}cm^{-2}$ between the upper edge of the valence band E_v and the level E_1 in the forbidden band, and is referred to as region 1. Region 2 between E_1 and E_2 corresponds to the middle portion of the silicon band gap and has the surface state density N_{st2} $ev^{-1}cm^{-2}$. Region 3 covers the energy between E_2 and E_c, the bottom edge of conduction band; its surface state density is N_{st3} $ev^{-1}cm^{-2}$.

In this chapter we will deal only with N-type silicon substrates, an extension to P-type substrate is simple. The substrate is assumed to be grounded, and the upper edge of the valence band $E_v = 0$ serves as reference potential. All potentials and energy levels are for convenience normalized to units in volt.

For simplicity, the surface states are assumed to be of acceptor-type, i.e., they are negatively charged when filled with electrons and neutral when empty. The fixed oxide charge, Q_o, is assumed to be located directly at the $Si-SiO_2$ interface.

First, the high frequency capacitance C pf/cm^2 of the MOS structure is calculated. For this purpose, the frequency is assumed to be so high

that the response of the surface states to the ac signal can be neglected.

To calculate the depletion layer width X_d, the depletion approximation (22) is used in this chapter. The carrier concentration n and p in depletion are assumed to be negligible besides the impurity concentration N_D of the silicon substrate.

The MOS system is in steady-state after applying the voltage ramp of Fig. 4, if the charge in the surface state fully responds to the voltage ramp, so that surface states with an energy $E > E_F$ are empty and state $E < E_F$ are filled. Otherwise the system is in non-steady-state.

2.1 Steady-state Condition

Figure 5 shows the band diagram of a practical MOS structure with a simplified surface state distribution and a fixed charge, Q_o, at the $Si-SiO_2$ interface. If a negative voltage V is applied, the system is in depletion, and

$$V = V_{ox} + \Phi_{ms} + \varphi_s \quad , \tag{2.1}$$

where V_{ox} is the voltage drop across the oxide, and φ_s the surface potential of the silicon substrate.

Using charge neutrality in the MOS structure,

$$Q_M + Q_D + Q_o + Q_t = 0 \quad , \tag{2.2}$$

where Q_M is the charge on the metal, $Q_D = qN_D X_d$ the charge in the depletion layer, and Q_t the charge of the electrons trapped in surface states. Q_t is either negative or zero, since the surface states are of acceptor-type.

The charge on the metal electrode coul/cm^2 is

$$Q_M = C_{ox}(V - \varphi_s - \Phi_{ms}) . \tag{2.3}$$

Integrating Poisson's equation twice and using the depletion approximation, the surface potential is

$$\varphi_s = -qN_D X_d^2/2\epsilon_s \,, \tag{2.4}$$

and the depletion layer capacitance

$$C_D = \epsilon_s/X_d. \tag{2.5}$$

The measured and normalized total capacitance is the series combination of C_{ox} and C_D,

$$\frac{C}{C_{ox}} = \frac{1}{1 + C_{ox}/C_D} = \frac{1}{1 + C_{ox} X_d/\epsilon_s} \,. \tag{2.6}$$

Equations (2.1 - 2.6) are valid for both steady- and non-steady-state conditions.

If the silicon Fermi level E_F is in region 3 at flat band condition with bias $V < V_{FB} < 0$, the charge in the surface states trapped for different values of the surface potential φ_s is according to Fig. 5:

$$Q_t = \begin{cases} -qN_{ST3}(E_F - E_2 + \varphi_s) - qN_{ST2}(E_2 - E_1) - qN_{ST1}E_1 & |\varphi_s| < |E_F - E_2| \\ -qN_{ST2}(E_F - E_1 + \varphi_s) - qN_{ST1}E_1 & |E_F - E_2| < |\varphi_s| < |E_F - E_1| \\ -qN_{ST1}(E_F + \varphi_s) & |E_F - E_1| < |\varphi_s| \,. \end{cases} \tag{2.7}$$

When E_F is in region 3 (Fig. 5a) or $|\varphi_s| < |E_F - E_2|$ (Fig. 5c), the relation

$$C_{ox}(V + qN_D X_d^2/2\epsilon_s - \phi_{ms}) + qN_D X_d - Q_o - qN_{ST3}(E_F - E_2 - qN_D X_d^2/2\epsilon_s) - qN_{ST2}(E_2 - E_1) - qN_{ST1}E_1 = 0 \tag{2.8}$$

is easily obtained from equations (2.2), (2.3), (2.4) and (2.7).

The normalized capacitance C/C_{ox} is calculated by solving eq. (2.8) for X_d and substituting it into eq. (2.6);

$$C/C_{ox} = \left\{ 1 + \frac{C_{ox}}{C_{ox} + qN_{ST3}} + \left[\left(\frac{C_{ox}}{C_{ox} + qN_{ST3}} \right)^2 + \frac{2C_{ox}^2 \left[C_{ox}(\phi_{ms} - V) - Q_o + qN_{ST3}(E_F - E_2) + qN_{ST2}(E_2 - E_1) + qN_{ST1}E_1 \right]}{qN_D\epsilon_s (C_{ox} + qN_{ST3})} \right]^{1/2} \right\}^{-1} . \tag{2.9}$$

Flat band voltage is obtained from eq. (2.8) by letting $X_d \to 0$,

$$V_{FB1} = \frac{qN_{st3}(E_F - E_2) + qN_{st2}(E_2 - E_1) + qN_{st1}E_1 - Q_o}{C_{ox}} + \Phi_{ms} \quad . \qquad (2.10)$$

For increasing N_{st3} and constant N_{st2}, N_{st1}, the ratio C/C_{ox} in eq. (2.9) becomes insensitive to a change of the applied bias V. Therefore most of the change of Q_M is balanced by a change of Q_t, and Q_D and C_D vary little.

The Fermi level E_F is located in region 2 near flat band condition if the donor concentration N_D is low (Fig. 5b); or for negative bias if the donor concentration N_D is high, i.e. $|E_F - E_2| < |\varphi_s| < |E_F - E_1|$ (Fig. 5d).

By calculating the depletion layer width X_d from equations (2.2), (2.3), (2.4), (2.7) and substituting into equation (2.6), the normalized capacitance

$$C/C_{ox} = \left\{ 1 - \frac{C_{ox}}{qN_{st2} + C_{ox}} + \left[\left(\frac{C_{ox}}{qN_{st2} + C_{ox}} \right)^2 + \right.\right.$$
$$\left.\left. + \frac{2C_{ox}^2 \left[C_{ox}(\Phi_{ms} - V) - Q_o + qN_{st2}(E_F - E_1) + qN_{st1}E_1 \right]}{qN_D \epsilon_s (qN_{st2} + C_{ox})} \right]^{1/2} \right\}^{-1} \qquad (2.11)$$

is obtained.

The flat band voltage is according to Fig. 5b,

$$V_{FB2} = \frac{qN_{st2}(E_F - E_1) + qN_{st1}E_1 - Q_o}{C_{ox}} + \Phi_{ms} \quad . \qquad (2.12)$$

When the applied bias assumes a more negative value, the silicon energy bands bend up further, and the surface potential φ_s becomes more negative. When $|E_F - E_1| < |\varphi_s|$ (Fig. 5e), the Fermi level E_F lies in region 1, and the normalized capacitance is

$$\frac{C}{C_{ox}} = \left\{ 1 - \frac{C_{ox}}{C_{ox} + qN_{st1}} + \left[\left(\frac{C_{ox}}{C_{ox} + qN_{st1}} \right)^2 + \frac{2C_{ox}\left[C_{ox}(\Phi_{ms} - V) - Q_o + qN_{st1}E_F \right]}{qN_D (C_{ox} + qN_{st1})} \right]^{1/2} \right\}^{-1} . \qquad (2.13)$$

Fig. 6 shows the C-V curves of a MOS structure for the inserted surface state distribution calculated at steady-state from equations (2.9), (2.11) and (2.13). Curve A is for a structure with a silicon

donor concentration $N_D = 5 \times 10^{16}$ cm^{-3}. At flat band, point a, and from a to b, Fermi level E_F is in region 3. A large surface state density N_{st3} responding to the voltage ramp relates to a slow change of X_d and C_D. Feature b to c corresponds to $E_F - E_2 < |\varphi_s| < E_F - E_1$ and E_F lies in region 2. A decrease of Q_M is responded by an increase of Q_t (less negative) and Q_D (more positive) (eq. (2.2)). X_d increases faster from b to c than from a to b, i.e. region 3. E_F for feature c to d is located in region 1, and most of the changing Q_M is offset by the changing Q_t; the increase of X_d is slowed down. To the left of point d, i.e. onset of strong inversion, $|\varphi_s| = -(E_g - 2E_F)$, the normalized capacitance is constant;

$$\frac{C}{C_{ox}} = \left\{ 1 + C_{ox} \left[\frac{2(2E_F - E_g)}{2N_D \epsilon_s} \right]^{1/2} \right\}^{-1} \qquad (2.14)$$

The applied voltage for point d is found from equations (2.2), (2.3) and (2.7):

$$V_{i1} = E_g - 2E_F + \phi_{ms} - \frac{2N_D}{C_{ox}} \left[\frac{2\epsilon_s (2E_F - E_g)}{2N_D} \right]^{1/2} - \frac{1}{C_{ox}} \left[Q_o - 2N_{st1} (E_g - E_F) \right] \qquad (2.15)$$

The C-V curve B in Fig. 6 corresponds to a silicon donor concentration of 5×10^{15} cm^{-3}. E_F is below E_2 at flat band condition, in region 2 from e to f, and in region 1 from f to g. The slope of curve B between e-f is larger than that of curve A between b-c. To obtain the same rate of changing Q_D, a larger rate of changing X_d is needed for sample B than for sample A.

For both sample A and B, $E_1 > E_g - E_F$ is assumed. Strong inversion happens when E_F is in region 1 (Fig. 5e), and also when E_F is located in region 2 for $E_1 < E_g - E_F$. The applied voltage at onset

$$V_{i2} = E_g - 2E_F + \phi_{ms} - \frac{2N_D}{C_{ox}} \left[\frac{2\epsilon_s (2E_F - E_g)}{2N_D} \right]^{1/2} - \frac{1}{C_{ox}} \left[Q_o - 2N_{st2} (E_g - E_1 - E_F) - 2N_{st1} E_1 \right], \qquad (2.16)$$

of strong inversion, is obtained from equations (2.2), (2.3) and (2.7).

2.2 Non-steady-state Condition

When the MOS structure is in steady-state, the surface states are in dynamic equalibrium with semiconductor conduction band; i.e., emission rate and capture rate of surface state are so large, that the states follow the changing applied voltage.

Under non-steady-state condition, the electron emission rate from surface states above the equilibrium Fermi level, E_F, is much less than their capture rate. Thus, the net rate of change is determined by the emission rate.

The Shockley-Read-Hall theory of recombination (28,29) shows the rate of electrons emitted from a distribution of surface states to be the product of the number of trapped electrons n_{sti} at the i^{th} state and the corresponding emission probability e_{ni}:

$$-\frac{dn_t}{dt} = \sum_i n_{sti}(t, E_{ti})\, e_n(E_{ti}) \tag{2.17}$$

with

$$e_n(E_{ti}) = v\sigma N_c\, e^{(E_{ti} - E_g)/kT}, \tag{2.18}$$

where n_{sti} is a function of time and energy level of the state, v the thermal velocity of electrons ($\simeq 10^7$ cm/sec at room temperature), σ the capture cross-section of the states, and N_c the effective density of states in the conduction band.

Since surface states are continuously distributed across the band gap, the sum in eq. (2.17) is replaced by an integral,

$$-\frac{dn_t}{dt} = \int_0^{E_g} n_{st}(t, E_t)\, e_n(E_t)\, dE_t. \tag{2.19}$$

The transition from steady-state to non-steady-state during the negative slope cycle (Fig. 4) occurs when the emission rate of the trapped electrons is too low to provide dynamic equilibrium between surface states and voltage ramp:

$$\left.\frac{dQ_t}{dt}\right|_{n.s.s.} < \left.\frac{dQ_t}{dt}\right|_{s.s.} . \tag{2.20}$$

When either $|\varphi_s| < |E_F - E_1|$ or E_F is in region 2:

$$\left.\frac{dQ_t}{dt}\right|_{s.s.} = \frac{qN_{st2}C_{ox}\alpha}{qN_{st2}+C_{ox}}\left\{1 - \frac{\epsilon_s}{(qN_{st2}+C_{ox})\left[\left(\frac{\epsilon_s}{qN_{st2}+C_{ox}}\right)^2 + \frac{2\epsilon_s(V_1-V)C_{ox}}{qN_D(qN_{st2}+C_{ox})}\right]^{1/2}}\right\}, \tag{2.21}$$

where $\alpha = |dv/dt|$ is the voltage ramping rate, and

$$V_1 \equiv \frac{1}{C_{ox}}\left[qN_{st2}(E_F - E_i) + qN_{st1}E_i\right] - Q_o/C_{ox} + \phi_{ms} .$$

The derivation of eq. (2.21) is in Appendix B.

When either $|\varphi_s| > E_F - E_1$ or E_F is in region 1:

$$\left.\frac{dQ_t}{dt}\right|_{s.s.} = \frac{qN_{st1}C_{ox}\alpha}{qN_{st1}+C_{ox}}\left\{1 - \frac{\epsilon_s}{(qN_{st1}+C_{ox})\left[\left(\frac{\epsilon_s}{qN_{st1}+C_{ox}}\right)^2 + \frac{2\epsilon_s(V_2-V)C_{ox}}{qN_D(qN_{st1}+C_{ox})}\right]^{1/2}}\right\}, \tag{2.22}$$

where $$V_2 \equiv \frac{1}{C_{ox}}(qN_{st1}E_F - Q_o) + \phi_{ms} .$$

In non-steady-state, the emission rate for a single state in the band gap follows from eq. (2.17):

$$-\frac{dn_{st}}{dt} = n_{st}(t, E_t)\, e_n(E_t) \tag{2.23}$$

with the solution,

$$n_{st}(t, E_t) = n_{st}(0, E_t)\, e^{-e_n(E_t)t}, \tag{2.24}$$

where $n_{st}(O,E_t)$ is the number of trapped electrons per unit area unit energy at onset of non-steady-state.

In equation (2.24)

$$\exp[-e_n(E_t)t] = \exp[-v\sigma N_c e^{(E_t - E_g)/kT} t]$$

is the non-steady-state occupancy of the states, its shape (Fig. 7) is similar to a Fermi-Dirac distribution. The states are empty above an energy $E_m(t)$, and full below $E_m(t)$.

Figure 8 illustrates the energy band diagram of a MOS structure in non-steady-state. Onset of non-steady-state (Fig. 8a) occurs at $t = 0$; E_F and $E_m(0)$ coincide at the interface. The states $E_F < E_t < E_m(t)$ are filled with electrons after time t, and the states $E_t > E_m(t)$ are empty (Fig. 8b). The derivation of $E_m(t)$ is given in App. C.

The charge of the trapped electrons in non-steady-state for E_F in region 2 is (see App. C)

$$Q_t(t) = -qN_{st1}E_1 + qN_{st2}E_1 + qkT\ln\{[e^{-E_{m2}(0)/kT} + (\frac{N_{st2}}{N_{st2}}kT(e^{E_1/kT}-1) - e^{E_1/kT})^{-1}]\exp[\frac{N_{st1}}{N_{st2}}\upsilon\sigma N_c(e^{(E_1-E_g)/kT} - e^{E_g/kT}) - \frac{\upsilon\sigma N_c}{kT}e^{(E_1-E_g)/kT}]t - (\frac{N_{st1}}{N_{st2}}kT(e^{E_1/kT}-1) - e^{E_1/kT})^{-1}\}, \quad (2.25)$$

$E_{m2}(0) = E_F - qN_DX_D^2/(2\epsilon_s)$ is the energy level E_F at the onset of non-steady-state (Fig. 8a), X_d is given by eq. (B.2).

At the onset of non-steady-state, differentiating eq. (2.25) results in:

$$\left.\frac{dQ_t(t)}{dt}\right|_{t=0} = qN_{st1}\upsilon\sigma N_c kT[e^{(E_1-E_g)/kT} - e^{E_g/kT}] - qN_{st2}\upsilon\sigma N_c e^{\frac{E_1-E_g}{kT}} + qN_{st2}\upsilon\sigma N_c e^{(E_{m2}(0)-E_g)/kT} \quad (2.26)$$

The corresponding applied voltage V(0) was obtained by equating eq. (2.21) and eq. (2.26), using a computer iteration method.

If non-steady-state occurs for $E_F - E_1 < |\varphi_s|$, then $E_m(t) < E_1$,

and $$Q_t(t) = qN_{st1}kT\ln[1-(1-e^{E_{m1}(0)/kT})\exp(-\upsilon\sigma N_c e^{-E_g/kT}t)] \quad (2.27)$$

and $$\left.\frac{dQ_t(t)}{dt}\right|_{t=0} = qN_{st1}\upsilon\sigma N_c kT(e^{(E_{m1}(0)-E_g)/kT} - e^{-E_g/kT}), \quad (2.28)$$

where $E_{m1}(0) = E_F - qN_D X_d^2/(2\epsilon_s)$, X_d is given by eq. (B.3).

In non-steady-state, when E_F was originally located in region 2, and moves after time t to region 1, the trapped electronic charge is the sum of the charges in region 2 and 1:

$$Q_t(t) = qN_{st2}E_1 + qN_{st2}kT\ln\{[e^{-E_{m2}(0)/kT} + (\frac{N_{st1}}{N_{st2}}kT(e^{E_1/kT}-1) - e^{E_1/kT})^{-1}] \times \exp[(\frac{N_{st1}}{N_{st2}}v\sigma N_c(e^{(E_1-E_g)/kT} - e^{-E_g/kT}) - \frac{v\sigma N_c}{kT}e^{(E_1-E_g)/kT})t] - (\frac{N_{st1}}{N_{st2}}kT \times (e^{E_1/kT}-1)e^{E_1/kT})^{-1}\} + qN_{st1}kT\ln\{1-(1-e^{-E_1/kT})\exp[-v\sigma N_c e^{-E_g/kT}(t-t_1)]\}, \quad (2.29)$$

where t_1 is the time taken for E_F to sweep from $E_{m2}(0)$ to E_1.

Comparing equations (2.7), (2.21), (2.22) and (2.25-2.29), dQ_t/dt and Q_t are functions of the applied voltage only in steady-state, and functions of time and voltage in non-steady-state.

The normalized capacitance in non-steady-state is obtained from equations (2.2-2.6);

$$\frac{C}{C_{ox}} = \left\{1 - \frac{2C_{ox}^2}{qN_D\epsilon_s}\left[\frac{Q_o + Q_t(t)}{C_{ox}} - \phi_{ms} + V\right]\right\}^{-1/2}. \quad (2.30)$$

Figure 9 shows the calculated C-V curves of a MOS structure, The voltage ramping rate for curve A is 10 v/sec. The structure is in steady-state from a to b, it enters non-steady-state at point b, and the trapped electrons cannot be emitted from the states as fast as E_F sweeps across the surface state levels. E_F is in region 2 for feature b to c, and in region 1 from c to d. The assumed surface state distribution is shown in the left upper corner.

Curve B shows the steady-state C-V curve for the same structure. E_F is in region 2 from a to e, and in region 1 from e to f. The onset of strong inversion happens at point f.

3. SAMPLE PREPARATION

Three silicon wafers were used. Two of them were N-type with <100> orientation, 5 to 10 Ω-cm resistivity. The third was N-type with <111> orientation, 0.5 to 1 Ω-cm resistivity. All of them were single crystal, and well polished mechanically and chemically.

The wafers were first degreased and etched, then thermally oxidized in dry oxygen atmosphere in a resistance heated horizontal furnace, shown in Fig. 10, for 1.5 hours at 1100°C to grow about 1600 Å of SiO_2. This oxide layer was etched off by hydrofluoric acid. The detali of this procedure is listed in App. E.

For sample 1 and 2, the final oxides were grown for one hour at 1050°C in the furnace used for the first oxidation mentioned above. Sample 3 was oxidized for one hour at 1100°C. The measured oxide thickness as a function of the growth time for dry oxidation in oxygen is plotted in Fig. 11 (27).

After oxidation, sample 2 was annealed in a resistance heated furnace (Fig. 12) for half an hour at 400°C in a hydrogen ambient.

The oxides at the sample backs were dissolved by etching with hydroflupric acid and rinsing with deionized water before metalization. The front surfaces were covered eith apizon wax which was later removed by boiling in trichloroethylene.

The metal contacts of sample 1 and 2 were made by depositing aluminum from a heated tungsten filament in a diffusion high vacuum system (Fig. 13) at 8×10^{-6} torr. The area of the front contact was 20.26×10^{-4} cm^{-2}.

The metal contact of sample 3 was made by evaporating aluminum at 10^{-6} torr in a Varian high vacuum system that was equipped with two sorption pumps, a titanium sublimation pump and a sputter ion pump for initial, intermediate and final pumping respectively. The area of the front contact was the same as that of sample 1 and 2.

4. MEASUREMENT OF SURFACE STATE DENSITY

4.1 Methods of Measurements

For evaluation of the surface state density at the Si-SiO_2 interface, several techniques have been developed measuring the capacitance- and conductance- voltage characteristics of the MOS structure (8-12).

In this thesis, the high frequency method and the quasi-static method were used. Their theory, procedure and merits are briefly discussed below.

4.1.1 The High Frequency Method

The high frequency method first used by Terman (8) yields the surface state density by comparison of the measured high frequency ($\geq$1MHz) C-V curve with the ideal curve. The capacitance is measured at such a high frequency that surface states cannot follow. Therefore, they do not contribute to the measured capacitance, but they distort the ideal C-V curve. The voltage difference between experimental and theoretical curves for a given capacitance is

$$\Delta V = -(Q_o + Q_t)/C_{ox}\,, \qquad (4.1)$$

where Q_t is the charge in surface states.

Differentiating eq. (4.1) with respect to the surface potential φ_s.

$$\frac{d(\Delta V)}{d\varphi_s} = -\frac{1}{C_{ox}}\frac{dQ_t}{d\varphi_s} = \frac{C_{ss}}{C_{ox}}\,, \qquad (4.2)$$

where C_{ss} is the surface state capacitance.

Since $$C_{ss} = q N_{ss} , \qquad (4.3)$$

the surface state density N_{ss} is obtained by

$$N_{ss} = \frac{q}{C_{ox}} \frac{d(\Delta V)}{d\varphi_s} . \qquad (4.4)$$

The advantages of this method is its simplicity of measurement and further, it covers a large portion of the band gap.

The accuracy limitations of this method have been discussed by Zaininger and Warfield (30). The most serious inaccuracy comes from the graphical differentiation of Δv with respect to φ_s. Another possible error is a measuring frequency chosen sot sufficiently high so that part of the surface states can still follow the signal.

4.1.2 The Quasi-Static Technique

The quasi-static technique measures the displacement current of the MOS device for a linear voltage ramp applied to the metal electrode. The circuit for performing this measurement is shown in Fig. 14, and the circuit diagram of the ramping generator is in Fig. 15.

When a linear ramping voltage $V(t) = V_1 \pm \alpha t$ is applied, the output voltage

$$V_o(t) = -RC(t)\frac{dV(t)}{dt} = \mp R\alpha C(t) \qquad (4.5)$$

is obtained, where α is the ramping rate, R is the shunt resistance across the operational amplifier in the electrometer, and C(t) the instantaneous capacitance of the MOS structure.

The displacement current is

$$i(t) = \mp \alpha C(t) , \qquad (4.6)$$

If the ramping rate is so low that the surface states can follow the applied voltage V(t), the equivalent circuit of Fig. 16 is applicable. The surface state capacitance is obtained from Fig. 16b as

$$C_{ss} = \frac{C_{ox}\, C(V)}{C_{ox} - C(V)} - C_D(\varphi_s), \tag{4.7}$$

where C is found by measuring the displacement current using the relationship between displacement current and measured capacitance, eq. (4.6). The surface potential is

$$\varphi_s = \int_{V_{acc}}^{V} \left(1 - \frac{C}{C_{ox}}\right) dV + K, \tag{4.8}$$

V_{acc} the applied voltage at strong accumulation, K an additive constant. $C_D(\varphi_s)$ is calculated theoretically (14), C_{ox} taken as saturation value of the high frequency C-V curve. The apparatus used for this measurement is shown in Fig. 20.

The surface state density N_{ss} is given by (13)

$$N_{ss} = \frac{C_{ox}}{q}\left[\frac{1}{\frac{C_{ox}}{C} - 1} - \frac{C_D}{C_{ox}}\right]. \tag{4.9}$$

Since the displacement current is small ($\sim 10^{-12}$ ampers), even a small leakage current can cause a big error. The equivalent circuit of the MOS capacitor with leakage and stray capacitance is plotted in Fig. 17, G is the leakage due to the MOS, C_{st} the stray capacitance, G_{st} the leakage due to the cables and all connections. To get the real MOS capacitance, the voltage ramp is applied in both positive- and negative-slope directions. The currents are measured while the probe touches the metal electrode,

$$\begin{aligned} i_+ &= C(t)\alpha + GV + C_{st}\alpha + G_{st}V \\ i_- &= -C(t)\alpha + GV - C_{st}\alpha + G_{st}V \end{aligned} \tag{4.10}$$

When the voltage ramp is applied in both directions without MOS structure, the measured currents give the stray capacitance and leakage,

$$i_{st+} = C_{st}\alpha + G_{st}V$$

$$i_{st-} = -C_{st}\alpha + G_{st}V \quad . \tag{4.11}$$

From equations (4.10) and (4.11), the MOS capacitance C(t) is calculated

$$C(t) = \frac{1}{\alpha}\left[\frac{i_+ - i_-}{2} - \frac{i_{st+} - i_{st-}}{2}\right] \quad . \tag{4.12}$$

Since thermal equilibrium is required for validity of this method, the sweep rate α is chosen as small as possible. Kuhn and Nicollian (17) found that sweep rate smaller than 100 mv/sec was required.

To obtain the additive constant K in eq. (4.8) matching of experimental and theoretical curves in strong accumulation was used by Berglund (9) and Kuhn (13). Lopez found the integrated total surface potential to be always less than 1.1 ev (31). He proposed an alternative way to obtain the additive constant K by determining the difference between the evaluated integral and 1.1 ev, and then divided by 2. This value was added to the measured surface potential, thus centering the measured range in the band gap.

4.2 Measurements of Surface State Densities

The surface state densities of sample 1 and 2 were measured employing the high frequency and the quasi-static methods. Due to a large leakage current in sample 3, only the high frequency method could be used, since it was found that the outersurface of oxide of sample 3

was contaminated by negative ions as discussed in Chapter 5.

Employing the quasi-static method, the oxide capacitance C_{ox} was found from the high frequency C-V curves. The quasi-static C-V curves were measured in the system shown in Fig. 14. The voltage ramping rate used for both sample 1 and 2 was 71 mv/sec, which was slow enough to assure equilibrium. To eliminate leakage current and stray capacitance, the displacement currents and leakage currents were measured for both directions of voltage ramping, and eq. (4.12) was used for calculation. The integration of the surface potential eq. (4.8) and the theoretical C_D v.s. φ_s curves were computer calculated. The additive constants K's were found by centering the measured range in the band gap. The results are shown in Fig. 18 and 19.

Employing the high frequency method, the 1 MHz capacitance was measured point by point according to Fig 20. The donor concentrations were estimated by using the ratio of the capacitances at strong accumulation C_{ox} to that at strong inversion C_{min} (32) or calculated from Lehovec's equation (33),

$$N_D = n_i \left(\frac{C_{ox} C_{min} A}{C_{ox} - C_{min}} \right)^2 \frac{kT}{q} \frac{4}{q n_i \epsilon_s} \ln\left(\frac{N_D}{n_i}\right), \qquad (4.13)$$

where n_i is the intrinsic carrier concentration, and A the area of the metal electrode.

The comparison between theoretical and experimental high frequency C-V curves and the graphical differentiations were done by computer.

The surface state densities measured by the high frequency method and that measured by the quasi-static method differed by factors of 1.5 to 10. Because of the mentioned limitated accuracy of the high frequency

method, the results obtained by the quasi-static method were preferred when applicable.

Figure 21 shows the surface state density of sample 3 measured by the high frequency method.

We recognize from Fig. 18,19 and 21 that the surface state distributions are not uniform. They are low at mid-gap, and high near the conduction and valence band edges.

5. EXPERIMENTAL RESULTS AND DISCUSSION

Hgih frequency C-V curves were plotted by an X-Y recorder at different temperatures with different voltage ramping rates. The measurement apparatus is shown in Fig. 22. The MOS structure was loaded in a Stathan temperature test chamber SD 30, its temperature was controlled to within $\pm 1^{o}C$ and read by a copper-constantan thermocouple. The frequency of the ac signal generated by the Boonton 71 AR L-C meter is 1 MHz, its magnitude 1.5mV.

5.1 Sample 1

Figure 23 and 24 show the recorded C-V curves of sample 1 at $300^{o}K$ and $248^{o}K$ respectively for directions of voltage ramping with negative and positive slopes. Figure 25 shows the MOS C-V curves for steady-state and non-steady-state calculated from the dynamic theory. The assumed surface state distribution shown in the left upper corner was obtained by modifying the measured surface state distribution shown in Fig. 18. In calculating the non-steady-state curve, a ramping rate of 4.4 V/sec was assumed.

5.1.1 C-V Curves at Room Temperature with Negative Voltage Ramping Slope

5.1.11 Ramping Rate 71 mV/sec

Comparing the negative slope voltage ramping part of curve B in Fig. 23 and the steady-state C-V curve calculated by using dynamic

theory as shown in Fig. 25, reasonable agreement is found.

Feature a to b of curve B in Fig. 23 corresponds to feature a to b of Fig. 25. The silicon Fermi level E_F is located in region 2 of the surface state distribution (Fig. 25). The emission of trapped electrons is fast enough to respond to the ramping voltage. Since the number of trapped electrons in region 2 is small, their emission is not able to fully balance the changing of charge on the metal electrode, Q_M. Thus, the depletion layer width X_d increases.

Feature b - c of curve B in Fig. 23 corresponds to b - c of Fig. 25; E_F lies in region 1. Since $N_{st1} > N_{st2}$, most of the changing charge on the metal is balanced by the emitted electrons, therefore the increase of X_d is slower than that of feature a - b.

From c to d the structure is in strong inversion, the measured capacitance a constant.

The agreement between curve B of Fig. 23 and the calculated steady-state C-V curve was poor, when the surface state distribution in Fig. 25 was determined employing the high frequency method. This proves the higher accuracy of the quasi-static method for samples with negligible leakage current.

5.1.12 Ramping Rate 4.4 V/sec

In Fig. 23, the structure for a negative ramping voltage of rate 4.4 V/sec is at steady-state from a to 1, and in non-steady-state and deep depletion from 1 to m. The measured capacitance is constant from m to n, while the theoretical curve in Fig. 25 shows deep depletion.

This discrepancy can be explained according to Pierret (34), Sah and Fu (35) by considering the generation of minority carriers in deep depletion which was neglected in the theory of Chapter 2. This generation rate (36) is

$$\frac{d(Q_t + Q_p)}{dt} = \frac{q n_i (X_d - X_{df})}{2\tau_o},$$

with Q_p the charge of minority carriers, n_1 the intrinsic carrier concentration, and X_{df} the depletion layer width in inversion for equilibrium. The depletion layer width progressively widens during the initial stage of non-steady-state to offset the changing metal charge, since the emission of trapped electrons is low. The increase of X_d corresponds to a decreasing capacitance C and an increasing carrier generation rate. With the ramping voltage going more negative, the generation rate within the semiconductor eventually becomes large enough to precisely balance the rate of the changing metal charge. While the generated minority carriers pile up at the $Si-SiO_2$ interface, the depletion layer width X_d is constant, and the capacitance saturates. A large ramping rate requires a wider depletion layer to generate the minority carriers necessary to balance the changing metal charge, and the measured capacitance is decreased.

5.1.13 Ramping Voltage Stops, $V = V_{min}$

The measured capacitance increases according to Fig. 23 (n-o) at the ramping voltage stop $V = V_{min}$, because the depletion layer continues generating minority holes, although the metal charge has stopped decreasing. The generated carriers pile up at the $Si-SiO_2$

interface decreasing the depletion layer charge Q_D, thereby reducing X_d and then increasing the measured capacitance C. When X_d decreases to a value of equal minority carrier generation and recombination rate, thermal equilibrium is achieved, and X_d becomes constant.

5.1.2 C-V Curves at 300 K With Positive Ramping Voltage Slope

The C-V curves show some anomalies for a positive slope ramping voltage.

The flat portion o to p of curve A in Fig. 22 is caused by injection of electrons from the silicon bulk to the Si-SiO_2 interface where they recombine with accumulated holes. Depletion layer charge Q_D and width X_d remain constant with changing metal charge. The constant capacitance corresponds to the amount of band bending required to provide the electrons for recombination with holes at the interface. An increasing ramping rate requires more electrons and less negative surface potential $\varphi_s = -qN_D X_d^2/(2\varepsilon_s)$; X_d decreases and the measured capacitance C increases.

At point p of Fig. 23 most of the holes in the inversion layer have been recombined, and the silicon goes into weak inversion; the capacitance increases. From p to q, a capacitance ledge is observed corresponding to part c - b of Fig. 25. It is due to filling of surface states N_{st1} with electrons in region 1 (15.16). Since this filling does not fully balance the changing metal charge, depletion layer charge Q_D and capacitance are slightly increasing. Goetzberger and Irvin (16) used this ledge to estimate the capture rate of electrons by surface states.

Feature q - a in Fig. 23 shows a rapid increase of the capacitance. The filling of surface states continues; however, it is not very important, since N_{st2} N_{st1}. Most of the changing metal charge is balanced by the rapidly decreasing Q_D and X_d.

5.1.3 C-V Curves at 248°K

Figure 24 shows C-V curves of sample at 248°K. A voltage ramping rate 71 mV/sec is sufficient to drive the device into non-steady-state.

A larger voltage ramping rate corresponds to a smaller capacitance as in Section 5.1.12. The saturation capacitance for a ramping rate of 4.4 V/sec at 248°K (fig. 24) is smaller than that at 300°K (Fig. 23), since the intrinsic carrier density n_1 at 248°K is smaller than that at 300 K. Therefore a larger X_d is needed at 248°K to generate sufficient minority carriers for balancing the changing metal charge.

The C-V curves of Fig. 24 for a positive voltage ramping slope show anomalies similar to Fig. 23 already explained in Section 5.1.2.

5.2 Sample 2

Figures 26 and 27 present the C-V curves at 300°K and 248°K for sample 2 after annealing with hydrogen for 0.5 hours. Its decreased surface state density is shown in Fig. 19. Figure 28 shows the corresponding calculated steady- and non-steady-state C-V curves for the inserted surface state distribution obtained by simplifying Fig. 19.

The C-V curves in Fig. 26 measured at a ramping rate 71 mV/sec agree reasonably well with the theoretical steady-state curve in Fig. 28. The capacitance tail (b-c) and the ledge (p-q) of Fig. 23 are not observed in Fig. 26 as the silicon is already in strong inversion before E_F enters region 1.

5.3 Sample 3

Figures 29 and 30 show the measured C-V curves of sample 3, and Fig. 31 the corresponding theoretical steady- and non-steady-state C-V curves. The surface state distribution inserted in Fig. 31 was obtained from Fig. 20 by assuming a simple step form that resulted in best agreement between experimental and theoretical C-V curves.

The capacitance in Fig. 30 first decreases when a negative slope ramping voltage is applied to the metal, and then it increases and becomes constant. This behavior is due to mobil ions on the outer oxide surface as suggested by Pierret and Small (37). Increasing the applied voltage in negative direction, negative ions on the outer oxide surface are rejected from the metal electrode, thereby increasing the depleted lateral surface area and surface generation. To compensate for this effect, the generation of the depletion layer and therefore the width X_d decreases, and the measured capacitance C increases.

6. CONCLUSIONS

This thesis confirms and extends the theory of dynamic charge current- and capacitance-characteristics in MOS structures with surface states. A three-step surface state distribution has been used as approximation of the measured distribution. Analytical solutions for the dynamic charge current- and capacitance-characteristics were obtained.

In steady-state, the emission of trapped electrons from surface states accounts for the reduction of the slopes in the C-V curves from the ideal ones. The charging and discharging of the high density surface states in region 1 of the surface state distribution explains the measured capacitance ledge. Reasonable agreement is found between experimental and theoretical steady-state C-V curves.

In non-steady-state, the trapped electron emission rate is not large enough to respond to the voltage ramping. Thus, the emission process is a function of time, and deep depletion is found in the calculated C-V curves. Deep depletion is observed in the experimental non-steady-state C-V curves; then the capacitance saturates (Fig. 23), because of generation of minority carriers in the silicon depletion layer.

For surface state distribution measurements, the high frequency method and the quasi-static method are described and used. Differences of factors of 1.5 to 10 have been observed in the surface state densities measured by these two methods. Since the quasi-static

method has a less limited accuracy, its results are preferred, when applicable to low leakage currents.

The increase of the non-steady-state capacitance in the deep depletion region (Fig. 29), when negative slope voltage ramp is applied, has been explained by negative ions moving on the outer oxide surface.

APPENDIX A. LIST OF SYMBOLS

A Area of metal electrode.

C Measured capacitance of MOS device.

C_D Silicon depletion layer capacitance.

C_{ox} Oxide capacitance.

C_{min} Minimum high frequency capacitance.

C_{ss} Total surface state capacitance at or below the equilibrium frequency.

E_c Energy level at the bottom edge of silicon conduction band.

E_F Fermi level of silicon.

E_{FM} Fermi level of metal.

E_i Energy level at the middle lf silicon band gap.

E_g Band gap of silicon.

E_t Energy level of surface state.

$E_m(0)$ Energy level E_t at which the non-steady-state starts.

$E_{m1}(0)$ Energy level E_t at which the non-steady-state starts when silicon Fermi level E_F is located in region 1 of surface state distribution.

$E_{m2}(0)$ Energy level E_t at which the non-steady-state starts when E_F lies in region 2.

$E_m(t)$ Psuedo-Fermi level for for surface states when the MOS device is in non-steady-state.

E_1 Energy level E_t which seperates region 1 nnd 2 in surface state distribution.

E_2 Energy level E_t which seperates region 2 and 3 in surface state distribution.

E_v Energy level at the upper edge of silicon valence band.

k Boltzmann constant.

K Additive constant in surface potential integration.

N_D Donor concentration.

N_C Effective density of states in the silicon conduction band.

N_{ss} Surface state density.

N_{st1} Surface state density in region 1 of surface state distribution.

N_{st2} Surface state density in region 2.

N_{st3} Surface state density in region 3.

q Magnitude of an elementary charge.

Q_D Charge in silicon depletion layer.

Q_M Charge on the metal electrode.

Q_o Fixed charge in oxide.

Q_t Surface state charge.

t Time.

T Absolute temperature of the MOS device.

V Applied dc voltage on the metal electrode.

v Electron thermal velocity.

V_{ox} Voltage drop across the oxide.

X_d Depletion layer width.

X_o Oxide thickness.

ϕ_{ms} Work function difference between metal and semiconductor.

φ_s Silicon surface potential.

ϵ_s Dielectric permitivity of silicon.

α Voltage sweeping rate.

ϵ_{ox} Dielectric permitivity of silicon dioxide.

APPENDIX B. DERIVATION OF $dQ_t/dt|_{ss}$

When either $|\varphi_s| < |E_F - E_1|$ or E_F is in region 2, from equations (2.4) and (2.7);

$$\left.\frac{dQ_t}{dt}\right|_{s.s.} = -qN_{st2}\frac{d\varphi_s}{dt}$$

$$= qN_{st2}\frac{qN_D X_d}{\epsilon_s}\frac{dX_d}{dV}\frac{dV}{dt}$$

$$= -\frac{q^2 N_{st2}\alpha N_D X_d}{\epsilon_s}\frac{dX_d}{dV} \qquad \text{(B.1)}$$

From eq. (2.2) to (2.7)

$$X_d = -\frac{\epsilon_s}{C_{ox}+qN_{st2}} + \left\{\left(\frac{\epsilon_s}{C_{ox}+qN_{st2}}\right)^2 + \frac{2\epsilon_s C_{ox}(V_1-V)}{qN_D(qN_{st2}+C_{ox})}\right\}^{1/2} \qquad \text{(B.2)}$$

Substituting eq. (B.2) into eq. (B.1), eq. (2.21) is obtained.

When E_F is in region 1,

$$X_d = -\frac{\epsilon_s}{C_{ox}+qN_{st1}} + \left\{\left(\frac{\epsilon_s}{C_{ox}+qN_{st1}}\right)^2 + \frac{2\epsilon_s C_{ox}(V_2-V)}{qN_D(qN_{st1}+C_{ox})}\right\}^{1/2}, \qquad \text{(B.3)}$$

and

$$\left.\frac{dQ_t}{dt}\right|_{s.s.} = -\frac{q^2 N_{st1}\alpha N_D X_d}{\epsilon_s}\frac{dX_d}{dV}, \qquad \text{(B.4)}$$

thus eq. (2.19) is obtained.

APPENDIX C. TRAPPED SURFACE STATE CHARGE $Q_t(t)$ WHEN E_F IS IN REGION 2 (Fig. 8b)

The energy $E_m(t)$ will be calculated above which the surface states are empty, and below which they are filled. From eq. (2.16) and (2.21);

$$-\frac{dn_t}{dt} = \int_0^{E_g} n_{st}(0, E_t)\, e^{-e_n(E_t)t}\, e_n(E_t)\, dE_t$$

$$= \int_0^{E_1} N_{st1} v\sigma N_c e^{(E_t - E_g)/kT}\, dE_t + \int_{E_1}^{E_m(t)} N_{st2} v\sigma N_c e^{(E_t - E_g)/kT}\, dE_t$$

$$= N_{st1} v\sigma N_c kT \left[e^{(E_1 - E_g)/kT} - e^{-E_g/kT}\right] + N_{st2} v\sigma N_c \times \left[e^{(E_m(t) - E_g)/kT} - e^{(E_1 - E_g)/kT}\right] \quad (C.1)$$

And

$$n_t = \int_0^{E_g} n_{st}(t, E_t)\, dE_t$$

$$= N_{st1} E_1 + N_{st2}(E_m(t) - E_1) \quad (C.2)$$

Differentiating eq.(c.2), the emission rate of the trapped electrons is

$$-\frac{dn_t}{dt} = -N_{st2}\frac{dE_m(t)}{dt} \quad (C.3)$$

By equating eq. (c.1) to eq. (c.3), (see Appendix D)

$$E_m(t) = -kT \ln\left\{\left[e^{-E_{m2}(0)/kT} + \left(\frac{N_{st1}}{N_{st2}} kT\left(e^{E_1/kT} - 1\right) - e^{E_1/kT}\right)^{-1}\right] \times \exp\left[\left(\frac{N_{st1}}{N_{st2}} v\sigma N_c\left(e^{(E_1 - E_g)/kT} - e^{-E_g/kT}\right) - \frac{v\sigma N_c}{kT} e^{(E_1 - E_g)/kT}\right)t\right] - \left(\frac{N_{st1}}{N_{st2}} kT\left(e^{E_1/kT} - 1\right) - e^{E_1/kT}\right)^{-1}\right\} \quad (C.4)$$

where $E_{m2}(0) = E_F - qN_D X_d^2/(2\epsilon_s)$, X_d is given by eq. (B.2). (Fig. 8a)

$$Q_t(t) = -qN_{st1} E_1 - qN_{st2}(E_m(t) - E_1) \quad (C.5)$$

Substituting eq. (c.4) into eq. (c.5), eq. (5.25) is obtained.

APPENDIX D. SOLUTION OF $E_m(t)$

Equating eq. (c.1) and (c.3),

$$-\frac{dE_m(t)}{dt} = \upsilon\sigma N_c e^{-E_g/kT} e^{E_m(t)/kT} + \frac{N_{st1}}{N_{st2}}\upsilon\sigma N_c kT\left[e^{(E_i-E_g)/kT} - e^{-E_g/kT}\right] - \upsilon\sigma N_c e^{(E_i-E_g)/kT} \quad . \tag{D.1}$$

Let $$A = \upsilon\sigma N_c e^{-E_g/kT}$$

$$B = \frac{N_{st1}}{N_{st2}}\upsilon\sigma N_c kT\left[e^{(E_i-E_g)/kT} - e^{-E_g/kT}\right] - \upsilon\sigma N_c e^{(E_i-E_g)/kT},$$

then eq. (D.1) becomes

$$-\frac{dE_m(t)}{dt} = A e^{E_m(t)/kT} + B \quad . \tag{D.2}$$

Let $y = e^{E_m(t)/kT}$, i.e. $E_m(t) = kT \ln y$, and

$$\frac{dE_m(t)}{dt} = \frac{kT}{y}\frac{dy}{dt} \quad .$$

Equation (D.2) becomes

$$\frac{dy}{dt} + \frac{B}{kT}y = -\frac{A}{kT}y^2 \quad .$$

Multiplying both sides by $-y^2$,

$$-\frac{1}{y^2}\frac{dy}{dt} - \frac{B}{kT}\frac{1}{y} = \frac{A}{kT} \quad .$$

Let $u = y^{-1}$, then $du/dt = -y^{-2}dy/dt$,

$$\frac{du}{dt} - \frac{B}{kT}u = \frac{A}{kT} \quad . \tag{D.3}$$

Solving the differential equation (D.3),

$$u(t) = c e^{Bt/kT} - A/B \tag{D.4}$$

is obtained.

The boundary condition is

$$u(0) = y^{-1}(0) = e^{-E_{m2}(0)/kT}$$

thus

$$C = e^{-E_{m2}(0)/kT} + A/B \tag{D.5}$$

and

$$e^{-\frac{E_m(t)}{kT}} = \left(e^{-E_{m2}(0)/kT} + A/B\right) e^{Bt/kT} - A/B \tag{D.6}$$

i.e.

$$E_m(t) = -kT \ln\left\{\left(e^{-E_{m2}(0)/kT} + A/B\right) e^{Bt/kT} - A/B\right\}$$

where $E_{m2}(0) = E_F - qN_D X_d^2/(2\varepsilon_s)$, X_d is given by eq. (B.2).

APPENDIX E. PREOXIDATION WAFER TREATMENT

A) Initial degreasing and etching

1) Ultrasonic cleaning with deionized water for 5 minutes.

2) Degreasing by heating in trichloroethylene, acetone and methanol successively each for 5 minutes.

3) Boiling in solution of deionized water, hydrogen peroxide (H_2O_2) and NH_4OH (4:1:1 by volume) for 10 minutes.

4) Boiling in solution of deionized water, hydrogen peroxide and hydrochloric acid (HCl) (4:1:1 by volume) for 10 minutes.

5) Etched by HF for 2 minutes.

6) Decanted and boiled in deionized water for 3 minutes.

7) Etched in HNO_3 for 5 minutes.

8) Decanted in deionized water.

B) Oxidation

The wafer is loaded into a resistance heated horizontal furnace and oxidized at 1100°C for 1.5 hours. The dry oxygen is at the atmosphere pressure, the flow rate is 2 liters per minutes.

C) Second cleaning

1) Ultrasonic cleaning in acetone for 5 minutes.

2) Decanted with deionized water.

3) Etched by HF.

4) Decanted by deionized water.

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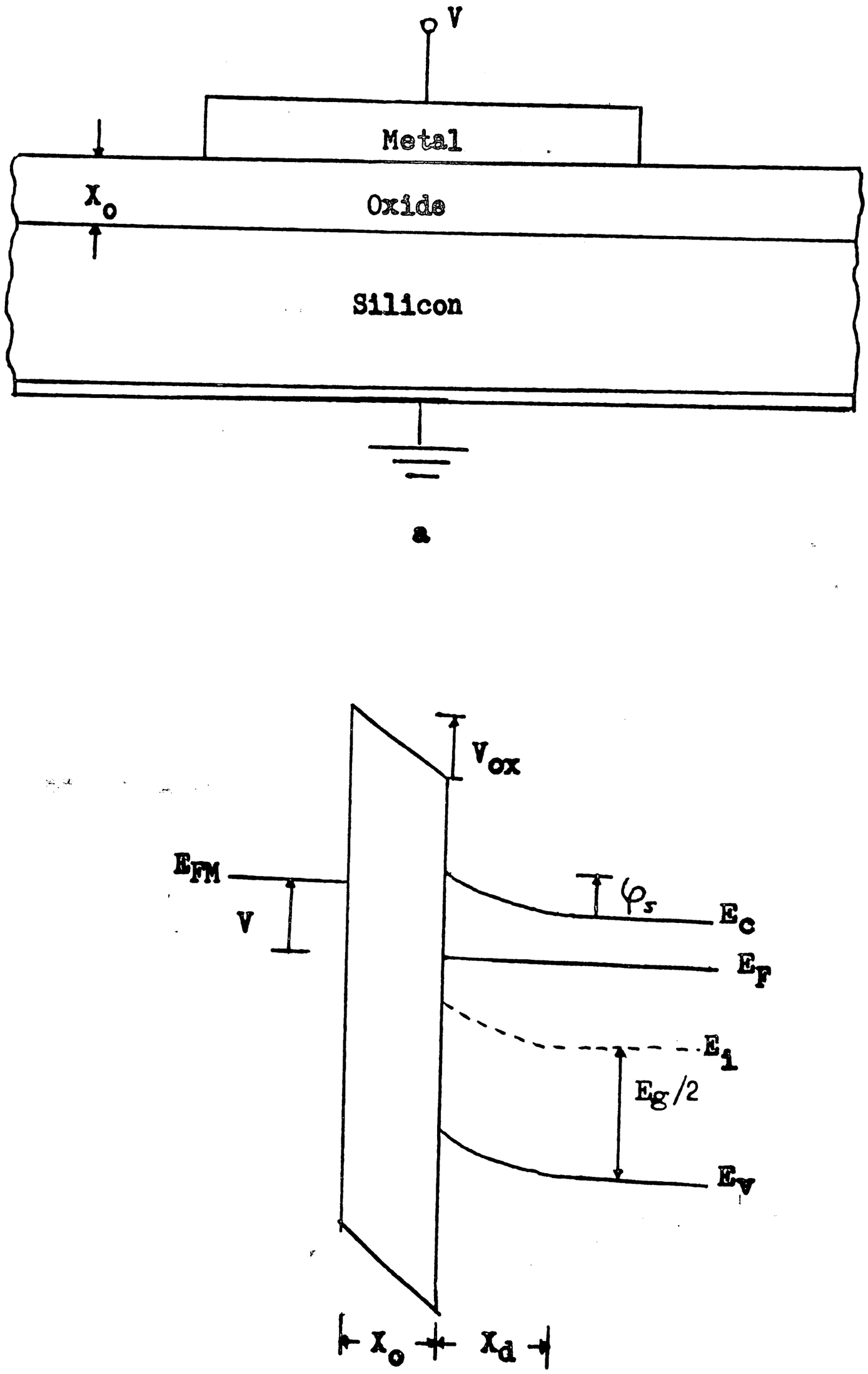

V
Metal
X_o
Oxide
Silicon
a
V_{ox}
E_{FM}
V
φ_s
E_c
E_F
E_i
$E_g/2$
E_v
X_o
X_d
b

Fig. 1

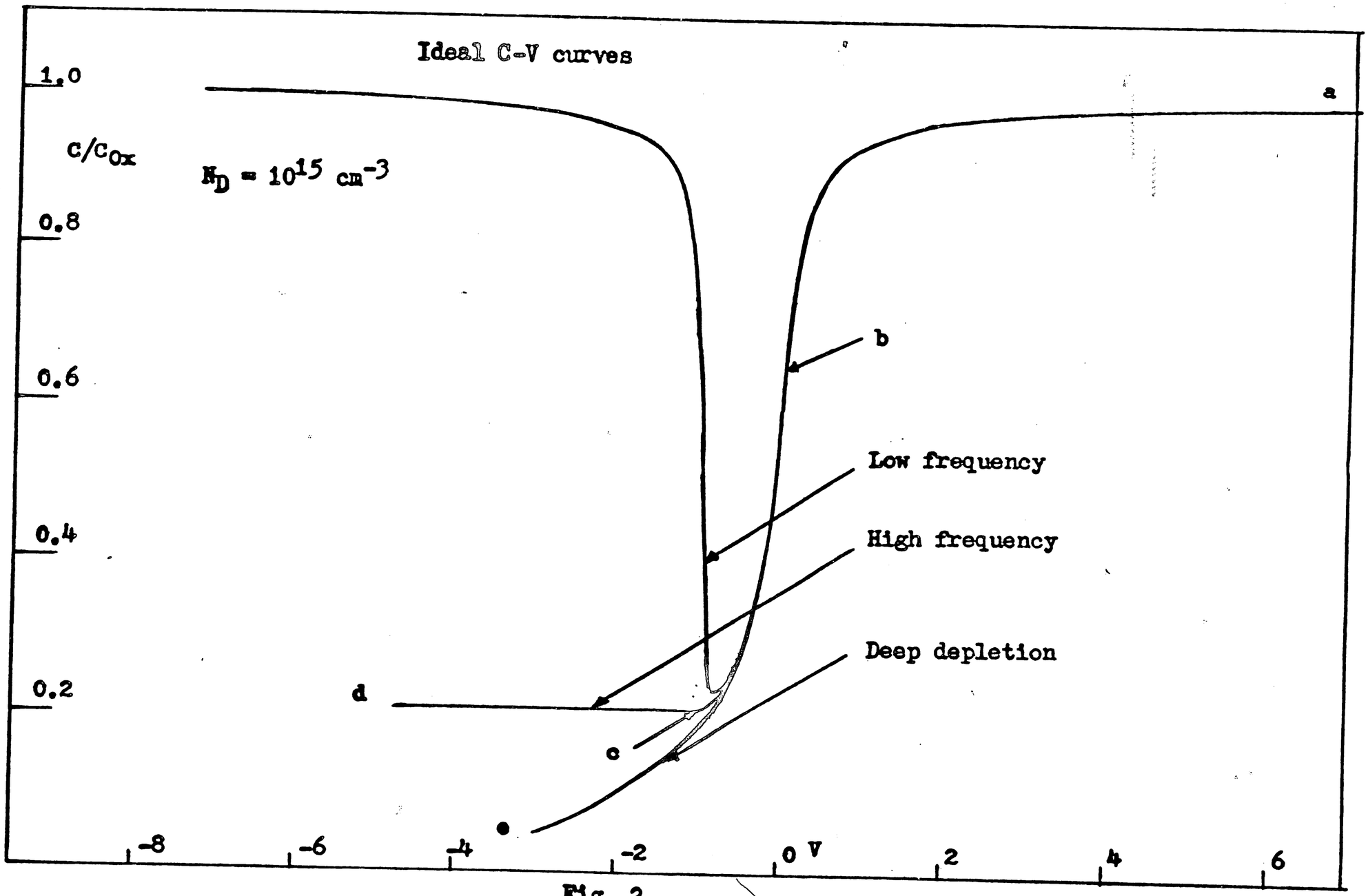
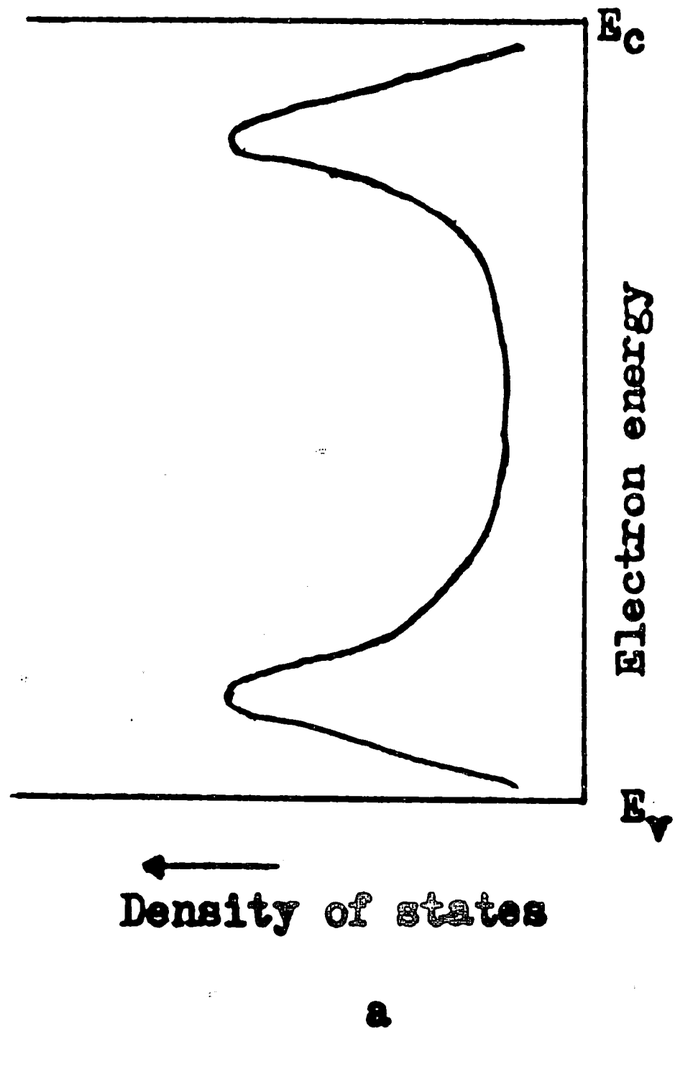
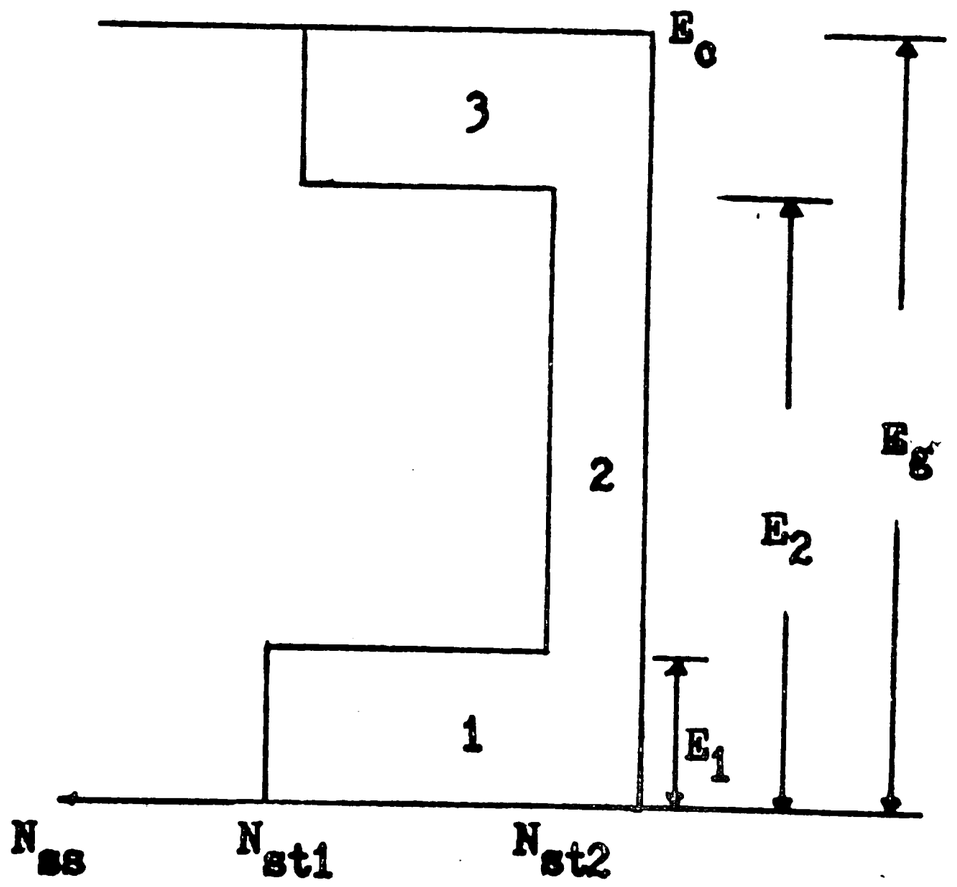

Ideal C-V curves
1.0
C/C_Ox
N_D = 10^15 cm^-3
0.8
0.6
0.4
0.2
a
b
Low frequency
High frequency
Deep depletion
d
c
-8
-6
-4
-2
0 V
2
4
6

Fig. 2


E_c
Electron energy
E_F
Density of states

a


E_c
3
2
1
E_g
E_2
E_1
N_{ss}
N_{st1}
N_{st2}

b

Fig. 3

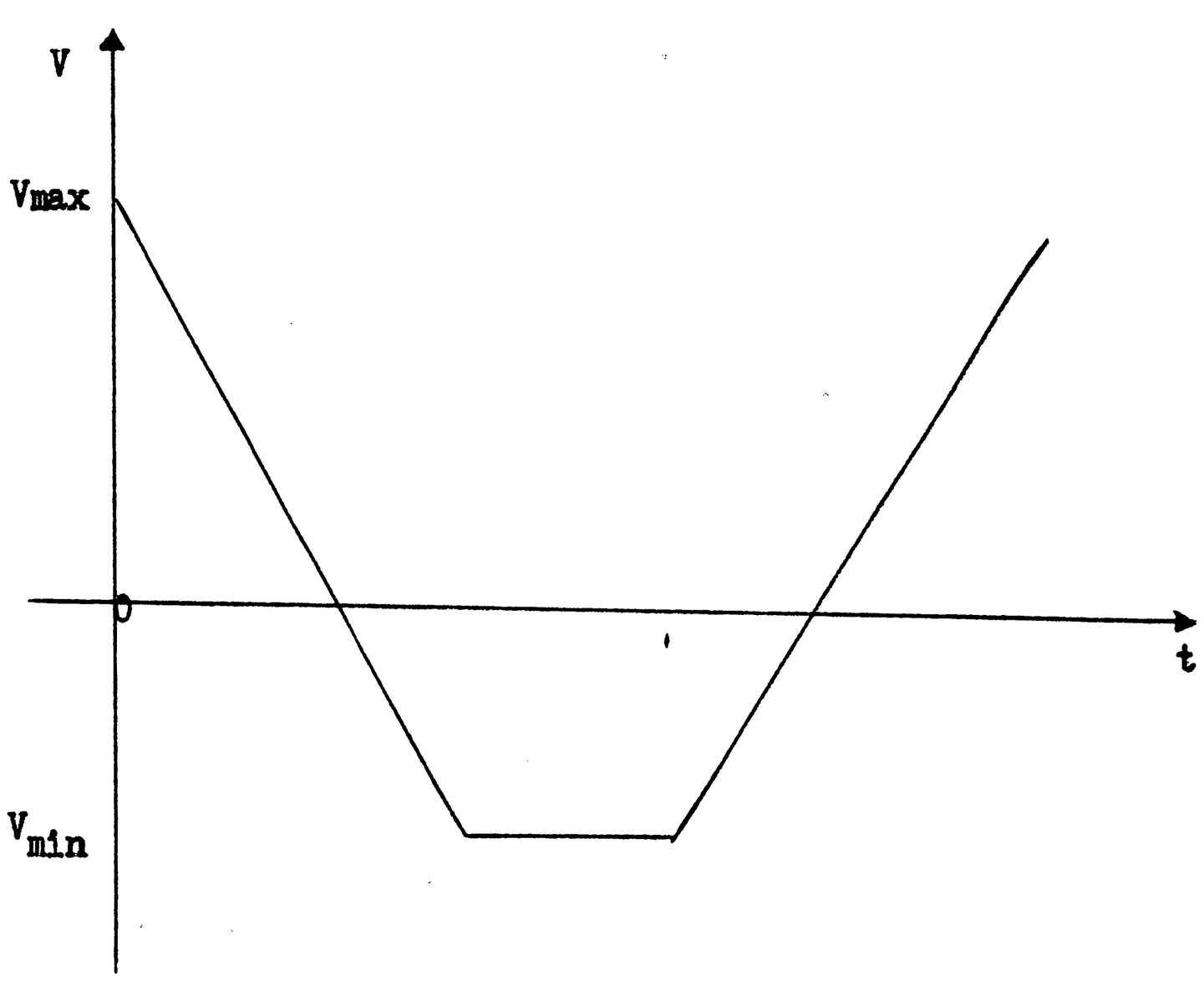
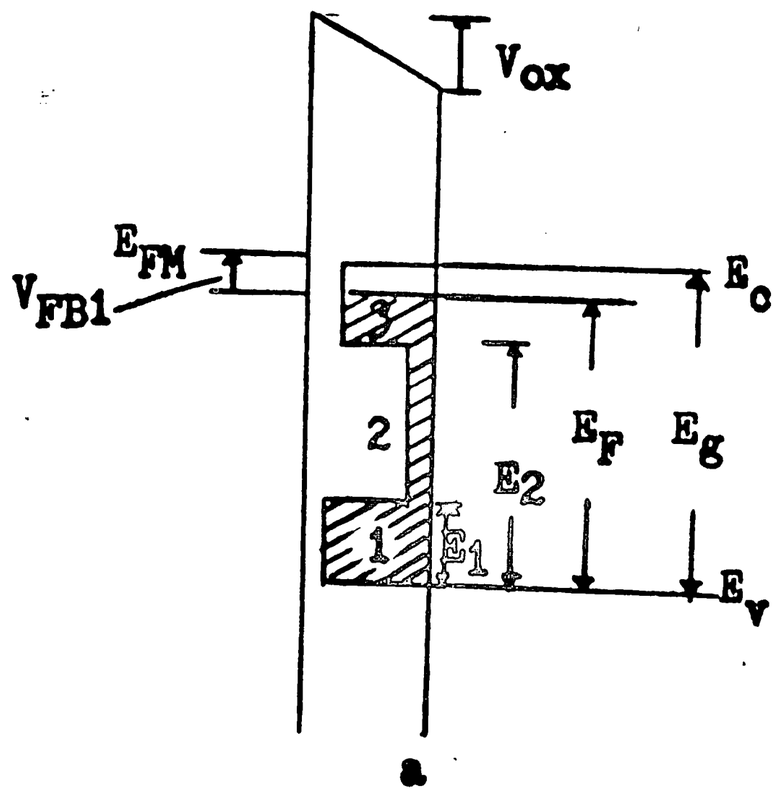
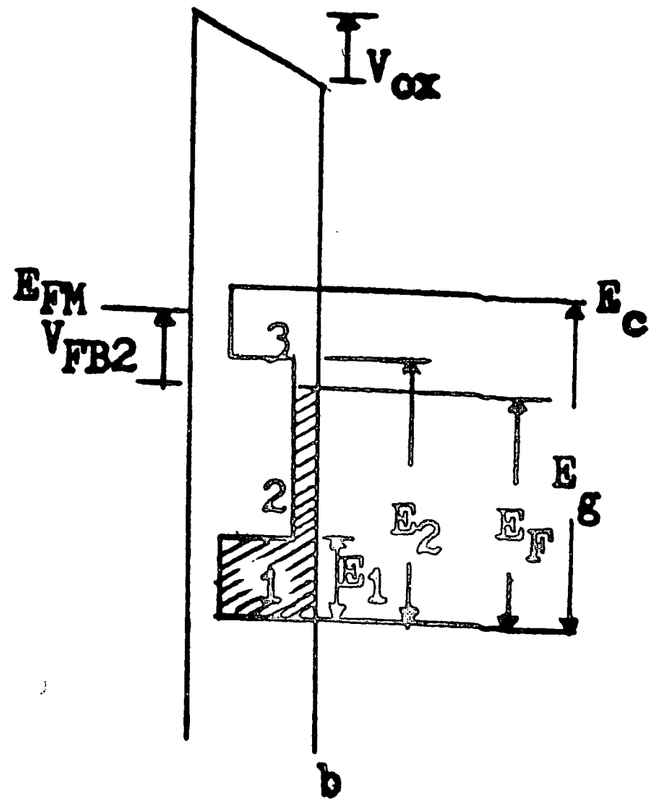
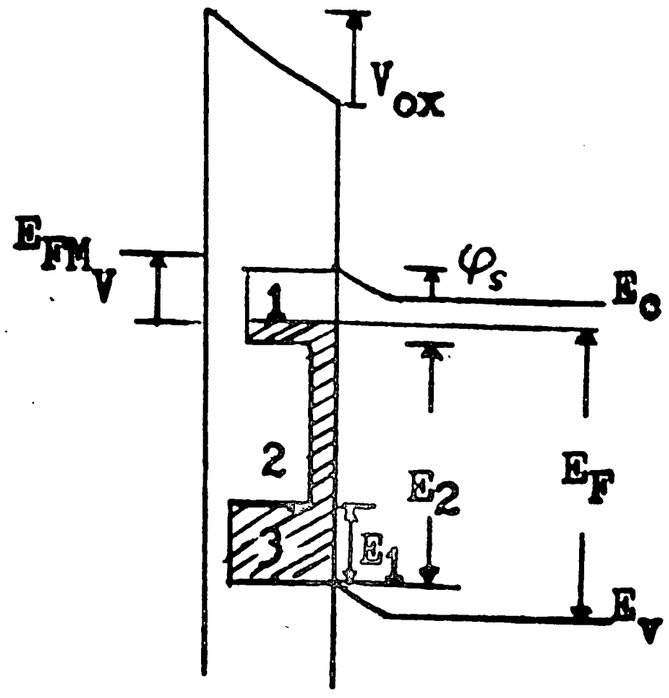
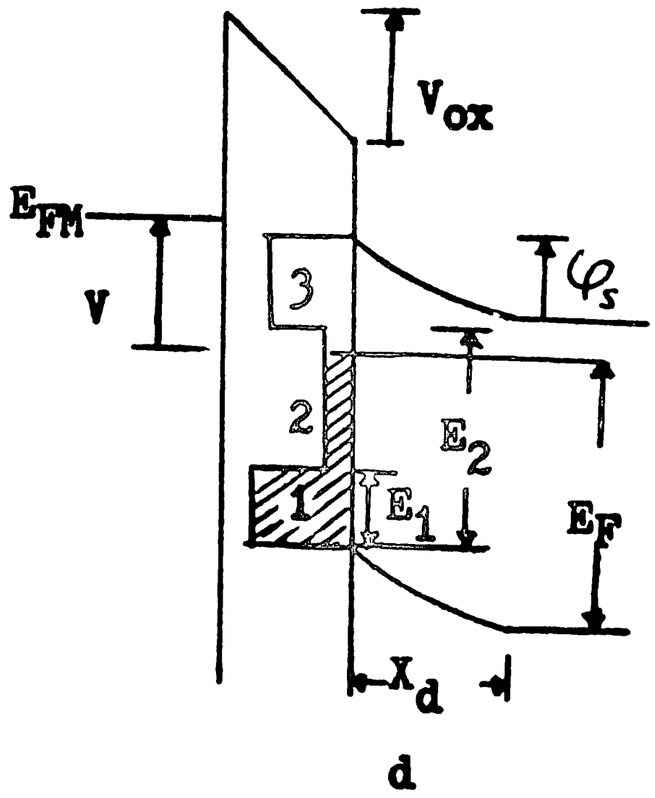


Fig. 4


V_{ox}
E_{FM}
V_{FB1}
E_c
E_F
E_g
E_2
E_1
E_v
3
2
1
a


V_{ox}
E_{FM}
V_{FB2}
E_c
E_g
E_2
E_F
E_1
3
2
1
b


V_{ox}
E_{FM}
V
φ_s
E_c
E_2
E_F
E_1
E_v
3
2
1
c


V_{ox}
E_{FM}
V
φ_s
E_2
E_1
E_F
X_d
3
2
1
d

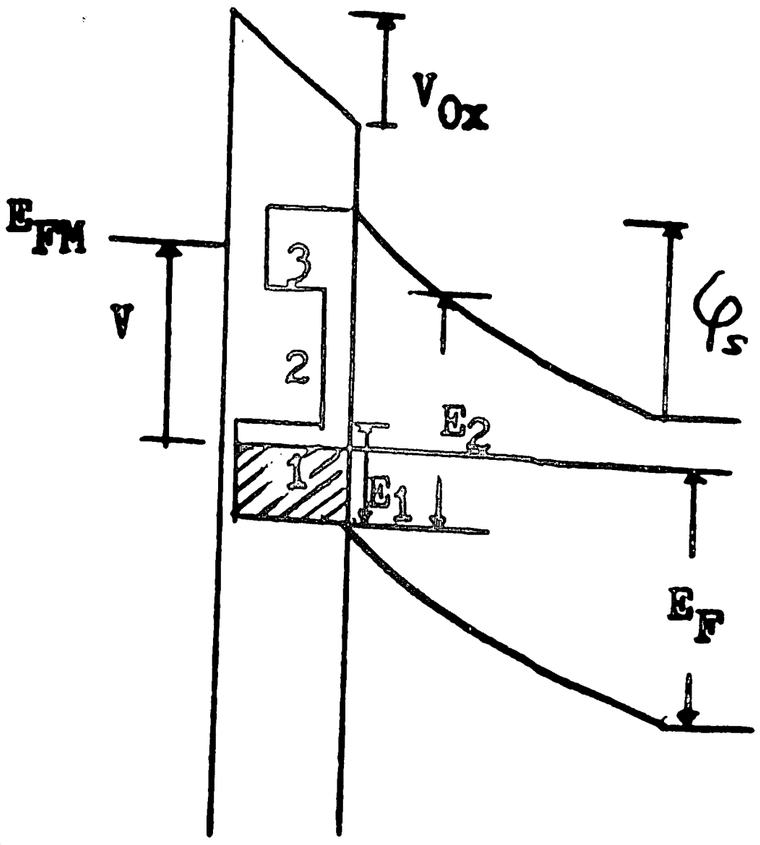
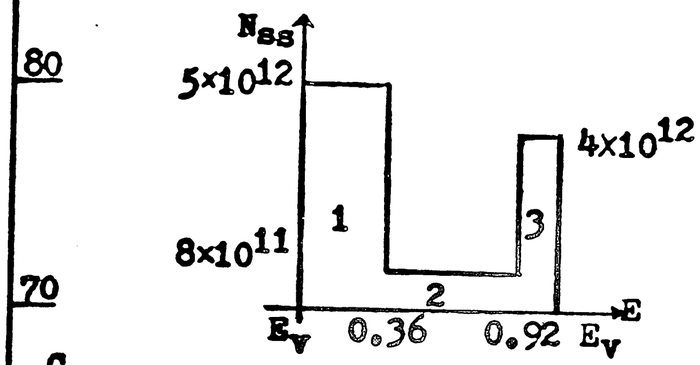

V_{ox}
E_{FM}
V
φ_s
E_2
E_1
E_F
3
2
1

Fig. 5



Oxide fixed charge = 2.5×10^{12} cm^{-2}

C_{ox} = 80 pf

ϕ_{ms} = 0.6 ev

Curve A $N_D = 5\times10^{16}$ cm^{-3}

Curve B $N_D = 5\times10^{15}$ cm^{-3}

Fig. 6

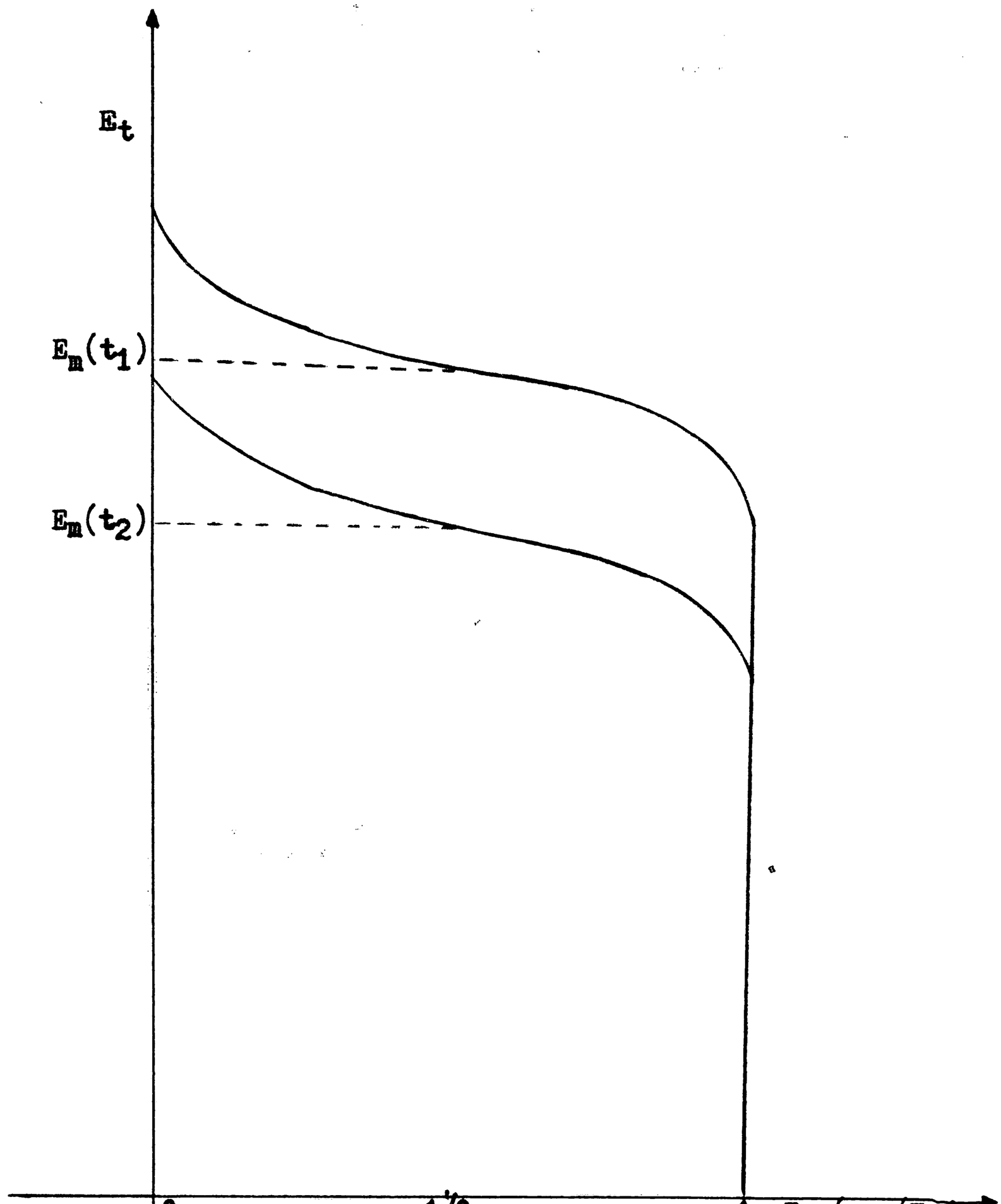
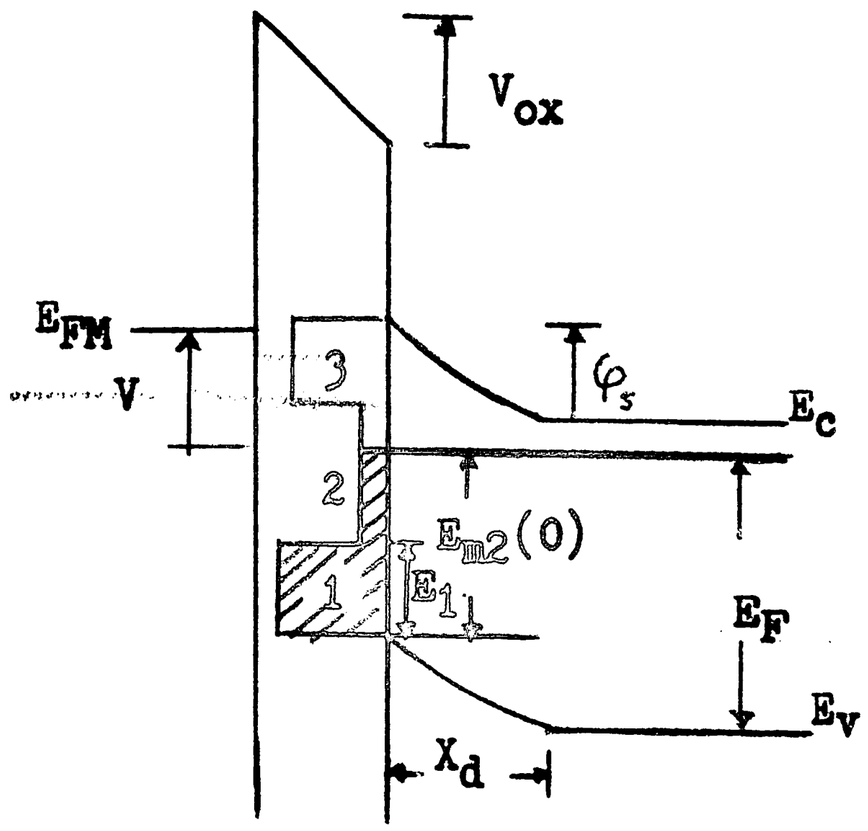
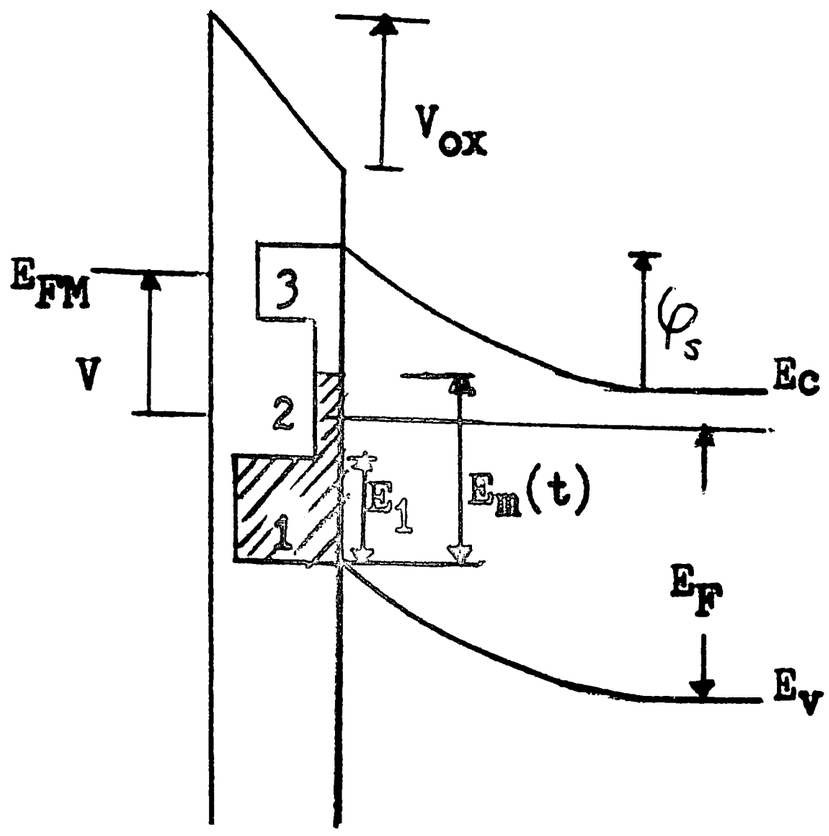


Fig. 7


V_{ox}
E_{FM}
V
3
2
1
$E_{m2}(0)$
E_1
φ_s
E_c
E_F
E_v
X_d

a


V_{ox}
E_{FM}
V
3
2
1
E_1
$E_m(t)$
φ_s
E_c
E_F
E_v

b

Fig. 8

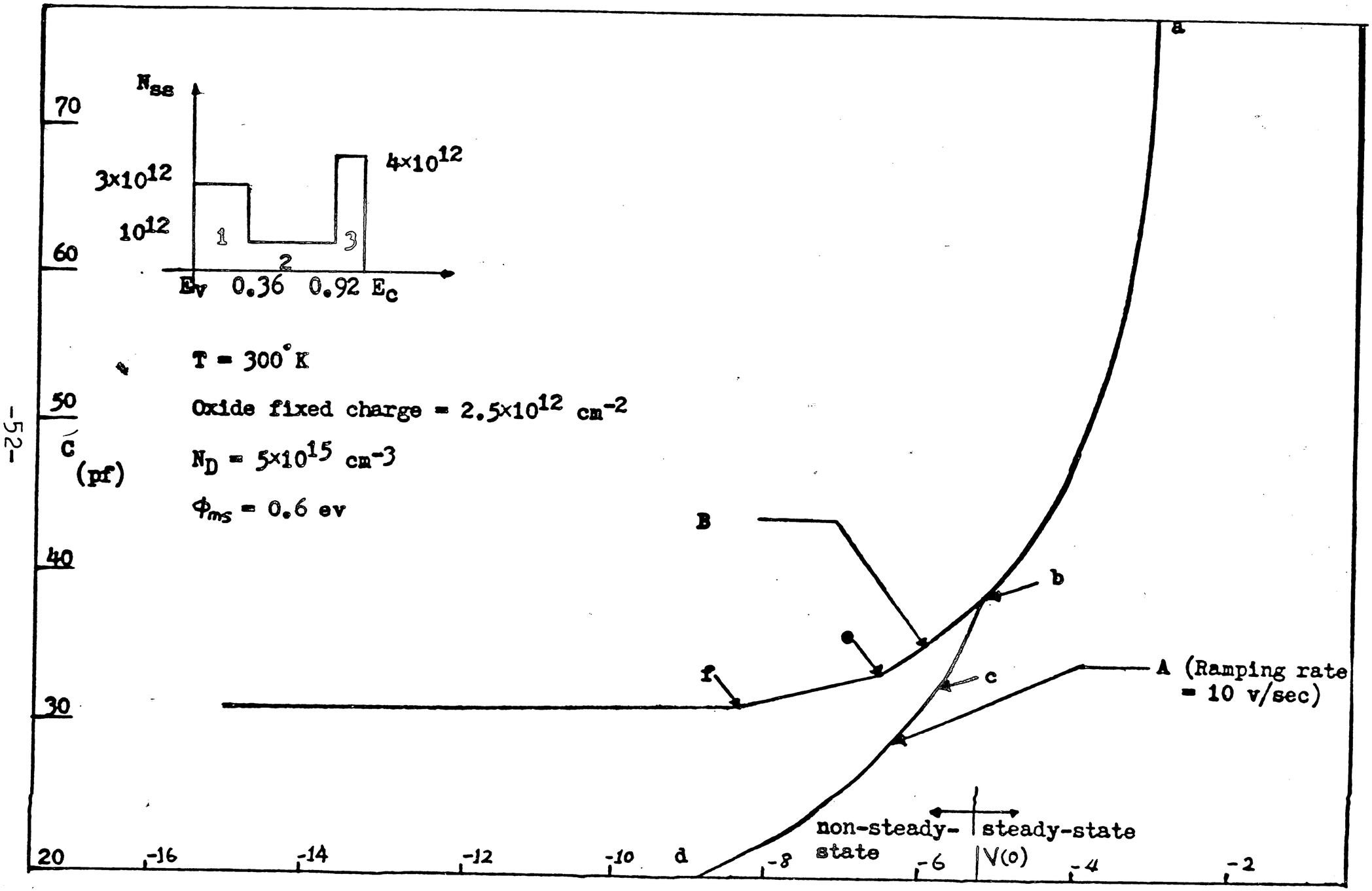

N_{ss}
70
3×10^{12}
4×10^{12}
10^{12}
60
1
2
3
E_v 0.36 0.92 E_c
T = 300° K
50
C (pf)
Oxide fixed charge = 2.5×10^{12} cm^{-2}
N_D = 5×10^{15} cm^{-3}
ϕ_{ms} = 0.6 ev
40
30
20
-16
-14
-12
-10
d
-8
-6
-4
-2
V(o)
non-steady-state
steady-state
a
b
c
d
e
f
A (Ramping rate = 10 v/sec)
B

Fig. 9

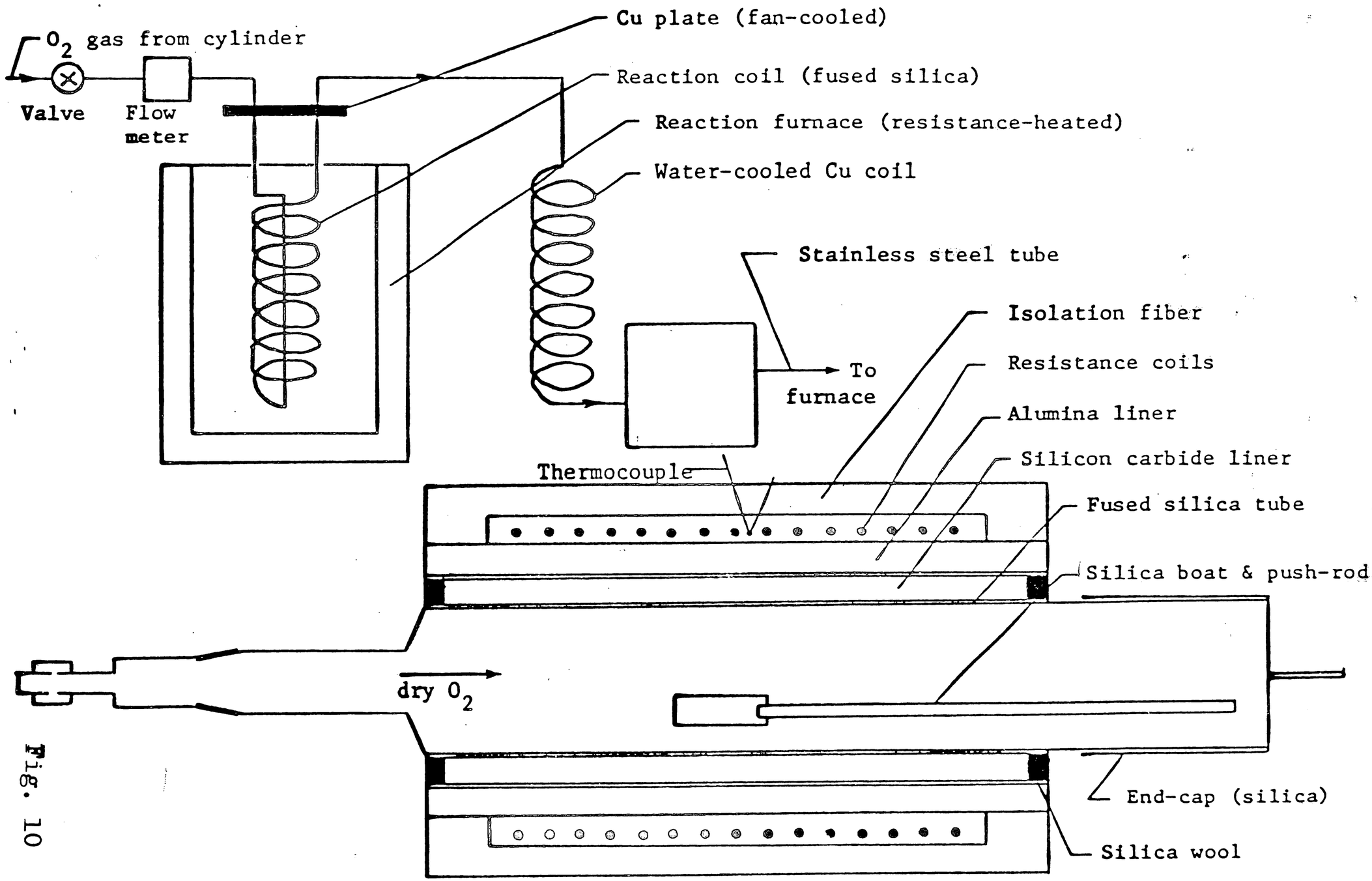

O_2 gas from cylinder
Valve
Flow meter
Cu plate (fan-cooled)
Reaction coil (fused silica)
Reaction furnace (resistance-heated)
Water-cooled Cu coil
Stainless steel tube
To furnace
Isolation fiber
Resistance coils
Alumina liner
Silicon carbide liner
Thermocouple
Fused silica tube
Silica boat & push-rod
dry O_2
End-cap (silica)
Silica wool

Fig. 10

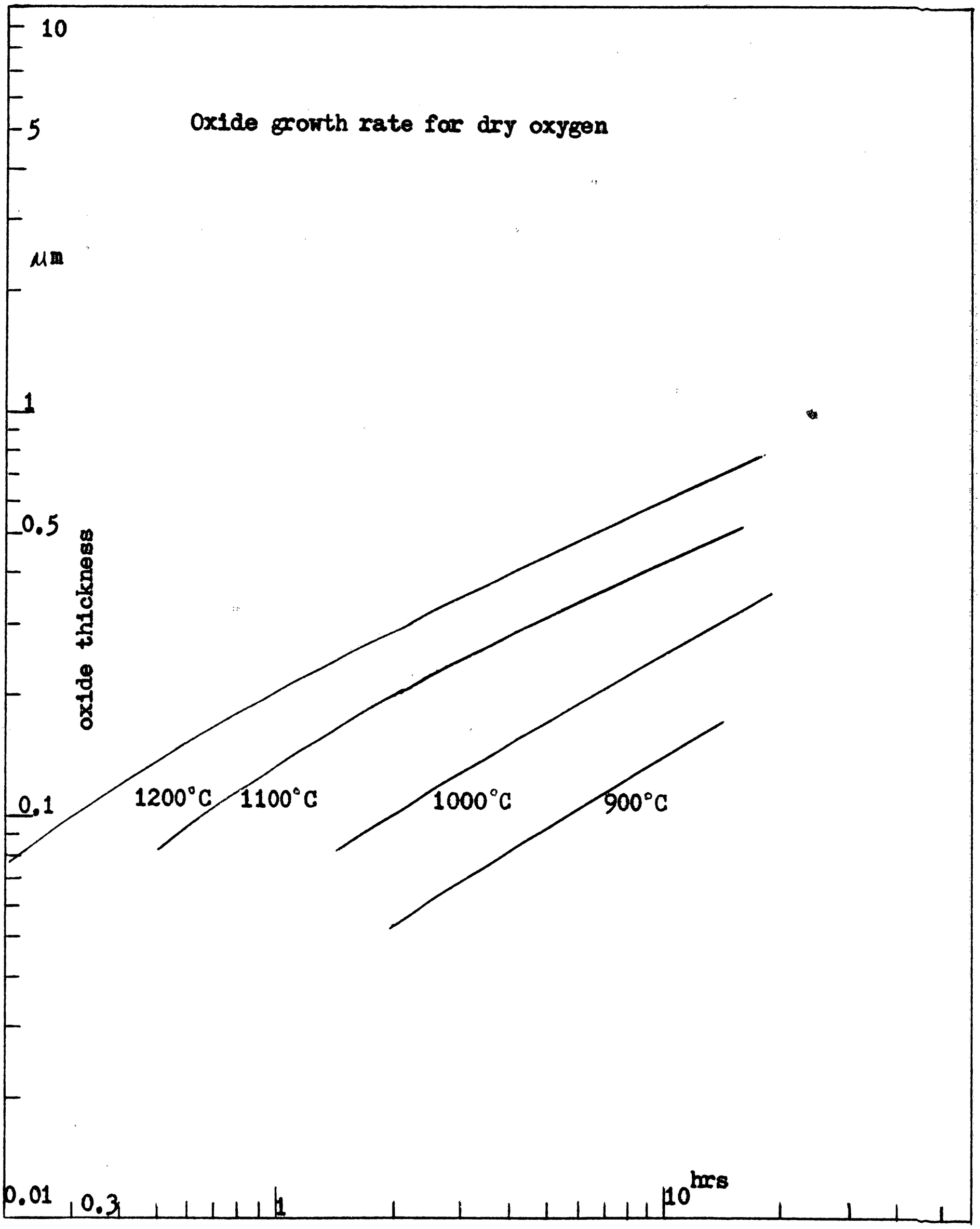

Oxide growth rate for dry oxygen
oxide thickness
10
5
1
0.5
0,1
μm
1200°C
1100°C
1000°C
900°C
0.01
0.3
1
10
hrs
oxidation time

Fig. 11

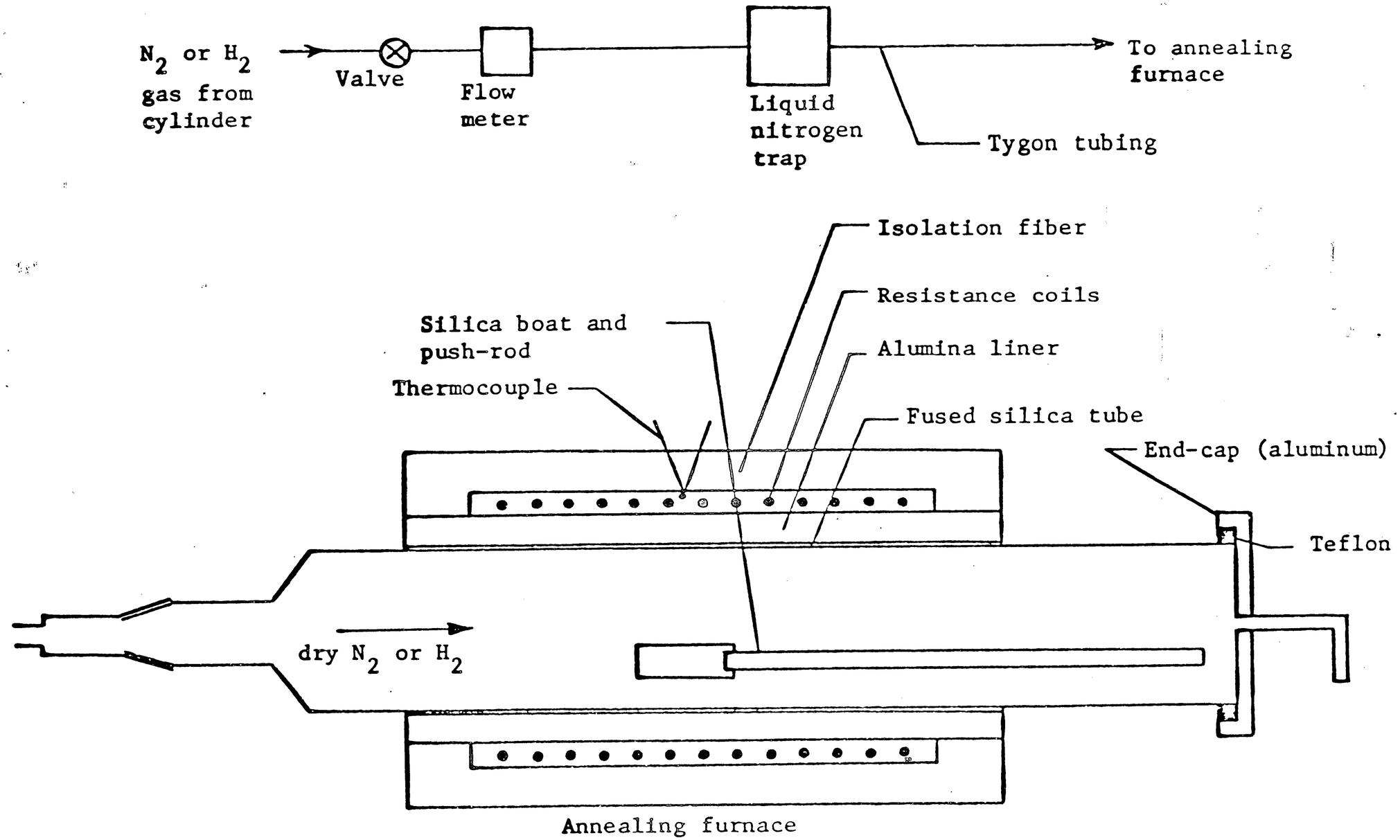

N_2 or H_2 gas from cylinder
Valve
Flow meter
Liquid nitrogen trap
To annealing furnace
Tygon tubing
Isolation fiber
Resistance coils
Silica boat and push-rod
Alumina liner
Thermocouple
Fused silica tube
End-cap (aluminum)
Teflon
dry N_2 or H_2
Annealing furnace

Fig. 12

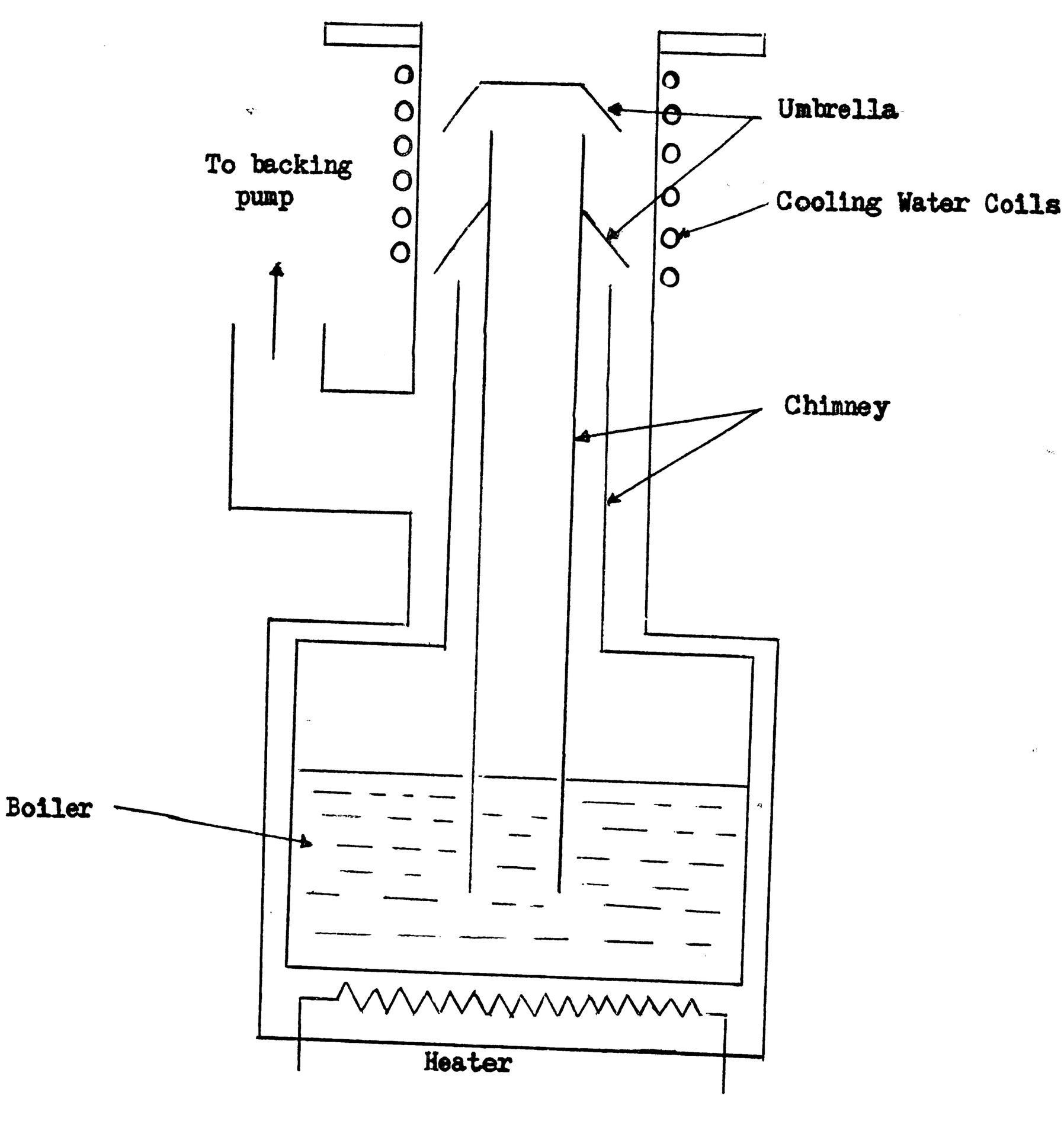
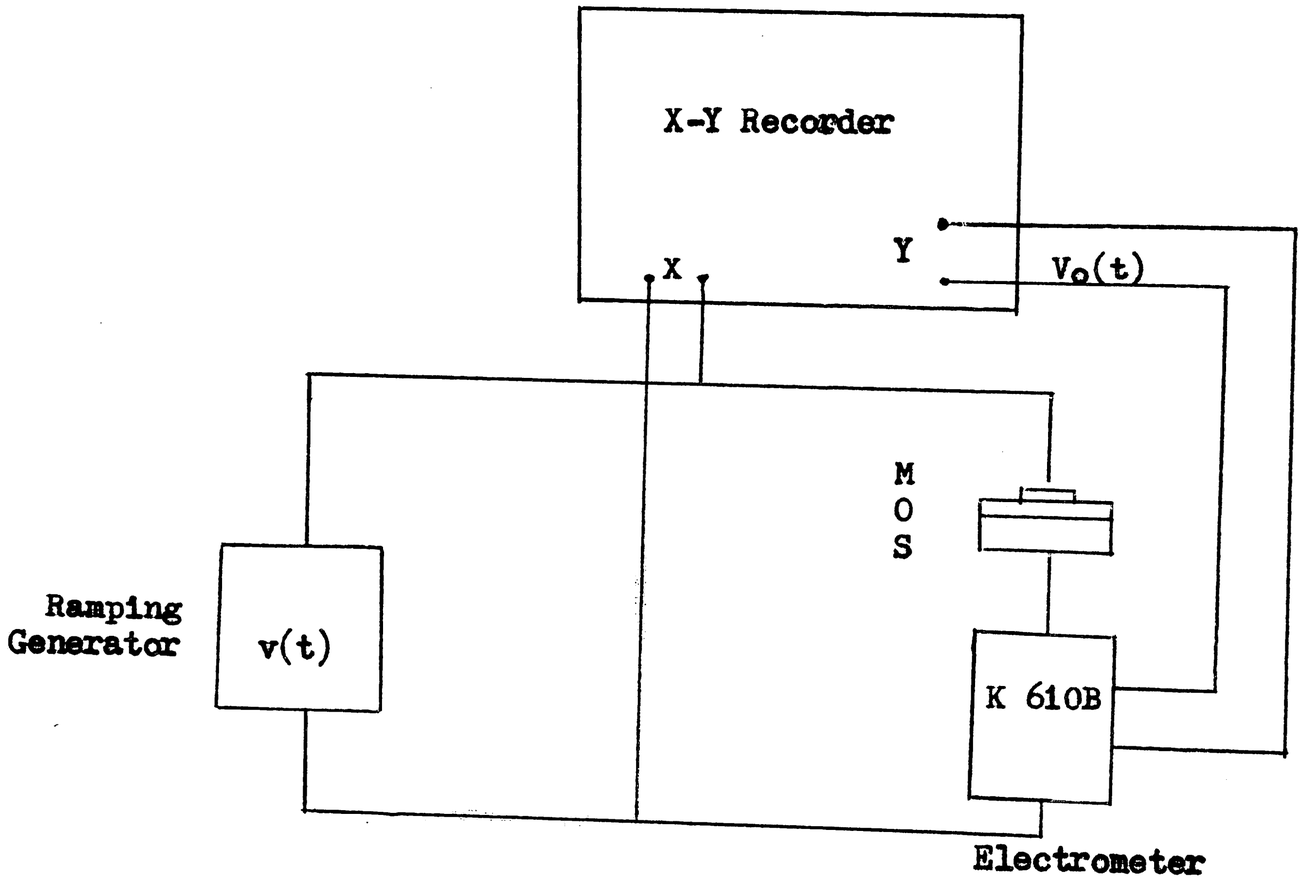

To backing pump
Umbrella
Cooling Water Coils
Chimney
Boiler
Heater

Fig. 13


X-Y Recorder
Y
X
$V_o(t)$
M
O
S
Ramping
Generator
v(t)
K 610B
Electrometer

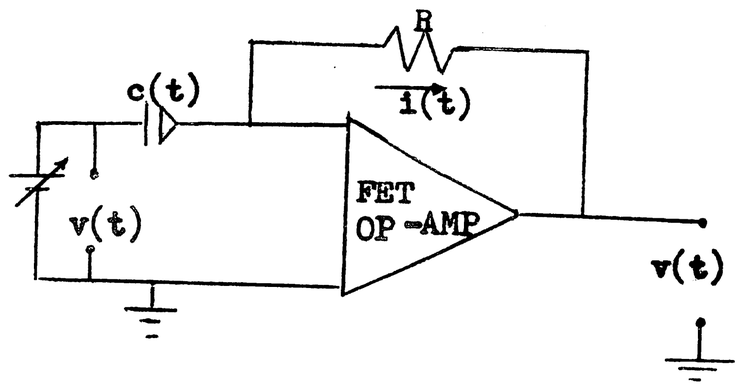

R
c(t)
i(t)
FET
OP -AMP
v(t)
v(t)

Fig. 14

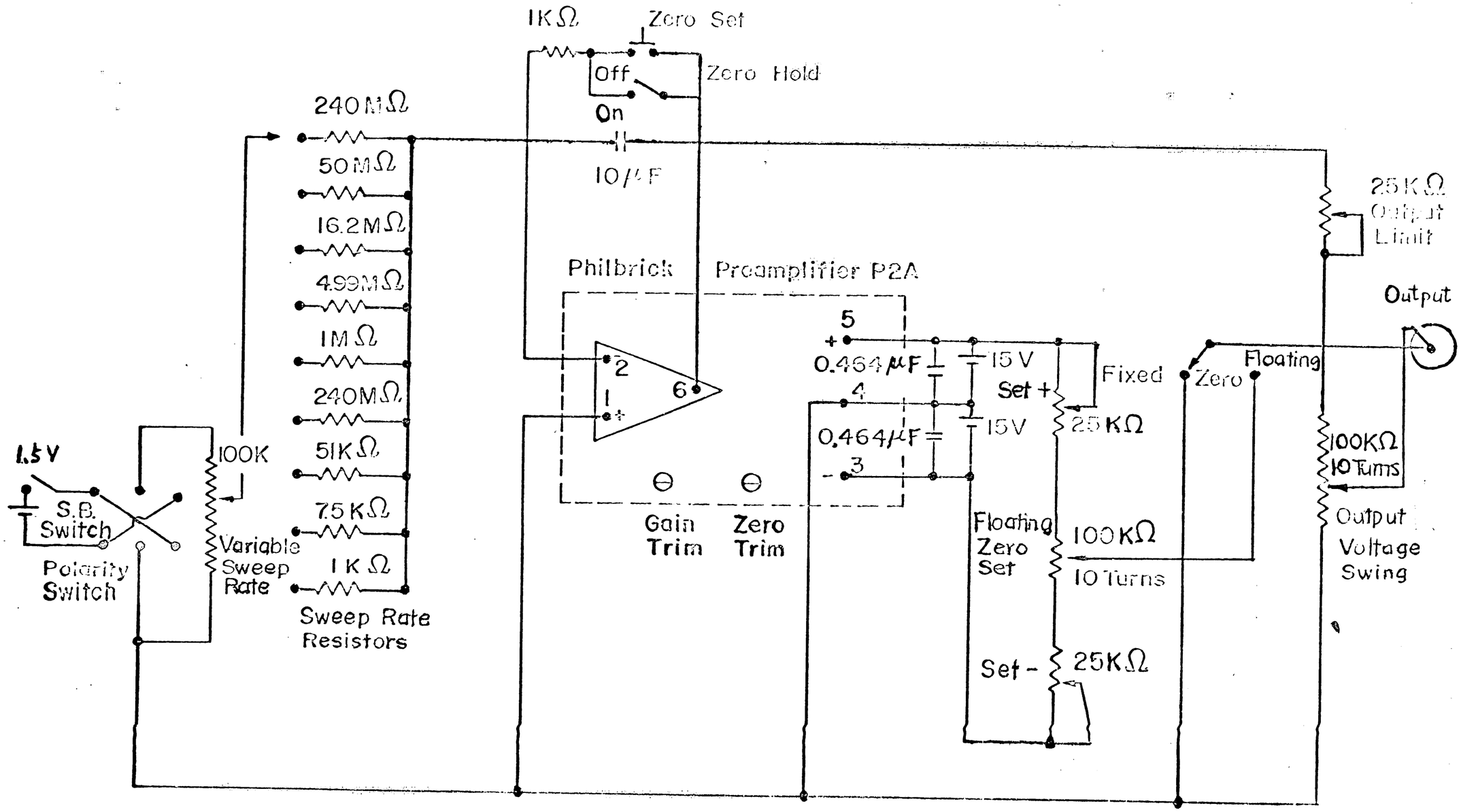


Fig. 15 RAMP GENERATOR

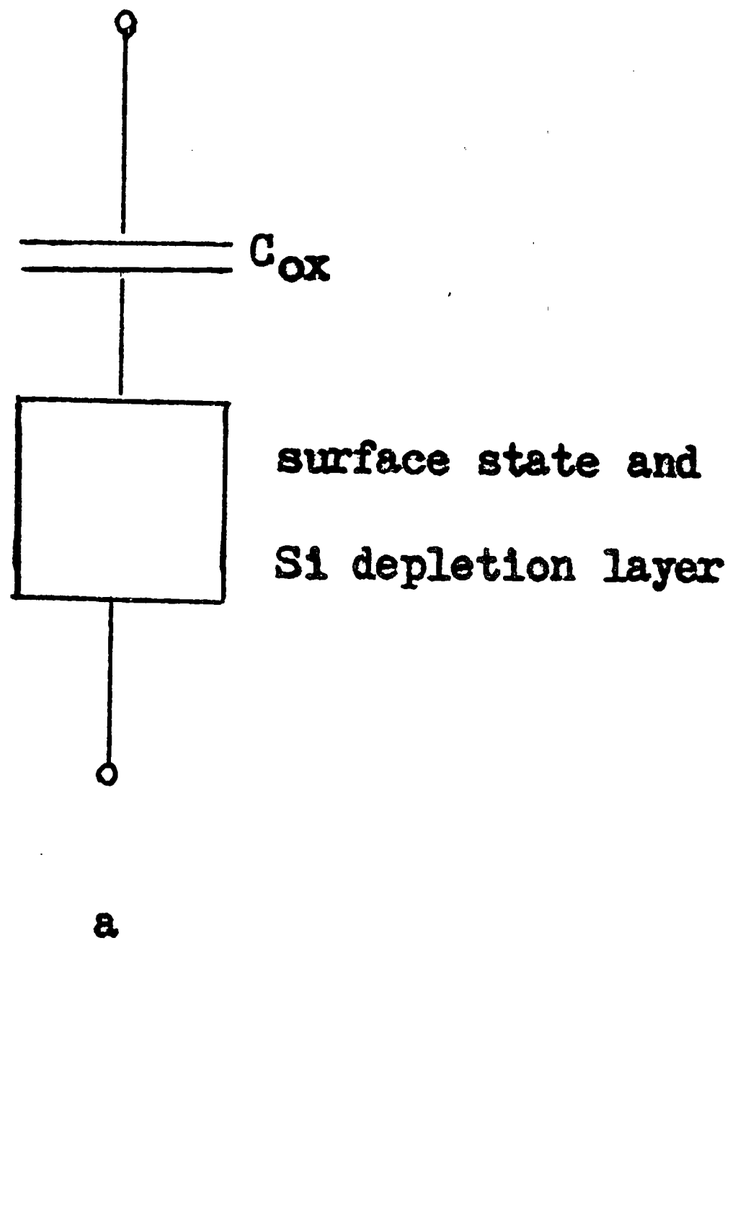


Fig. 16

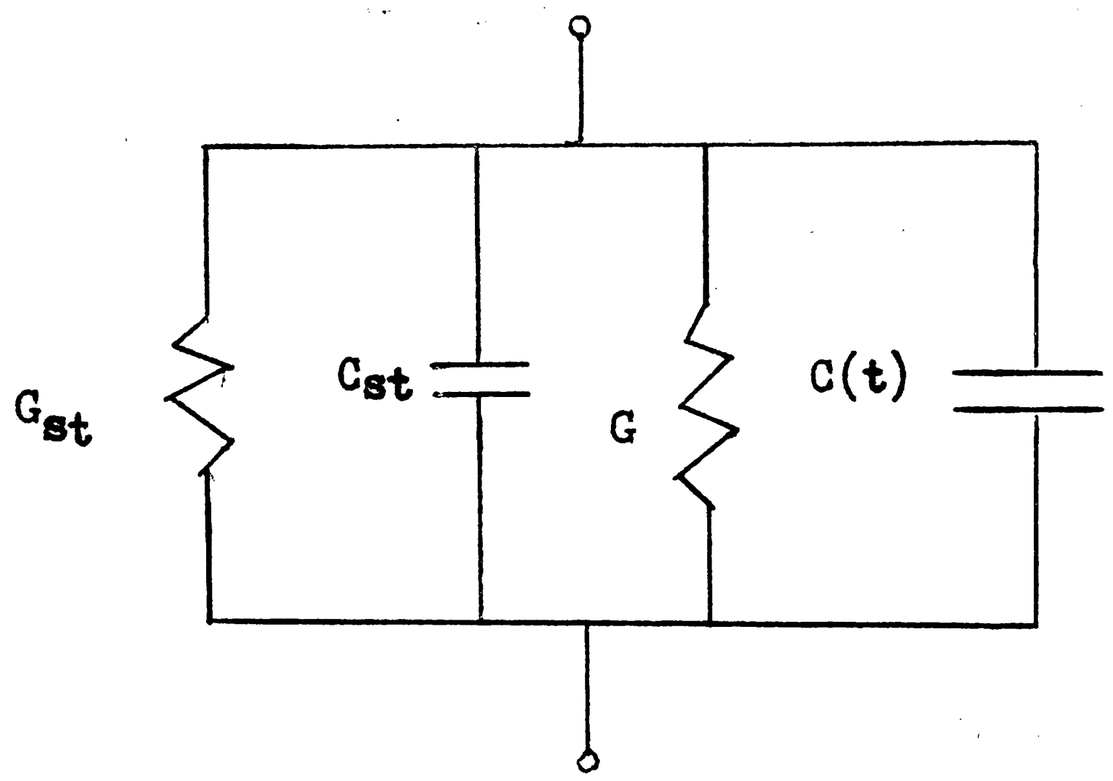


Fig. 17

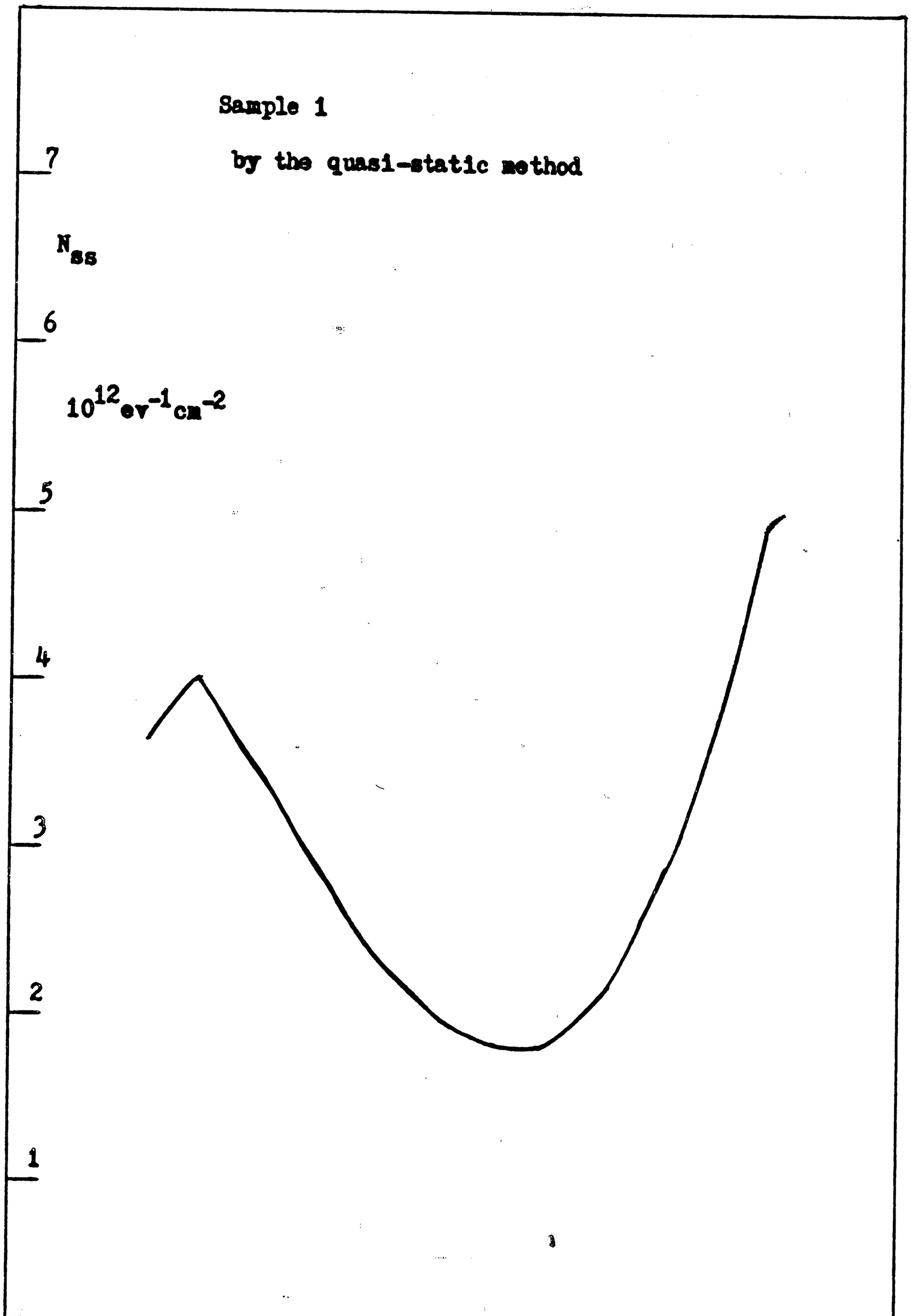

Sample 1
by the quasi-static method
N_{ss}
$10^{12} ev^{-1} cm^{-2}$
7
6
5
4
3
2
1
E_v
0.2
0.4
0.6
0.8
1.0 E_g

Fig. 18

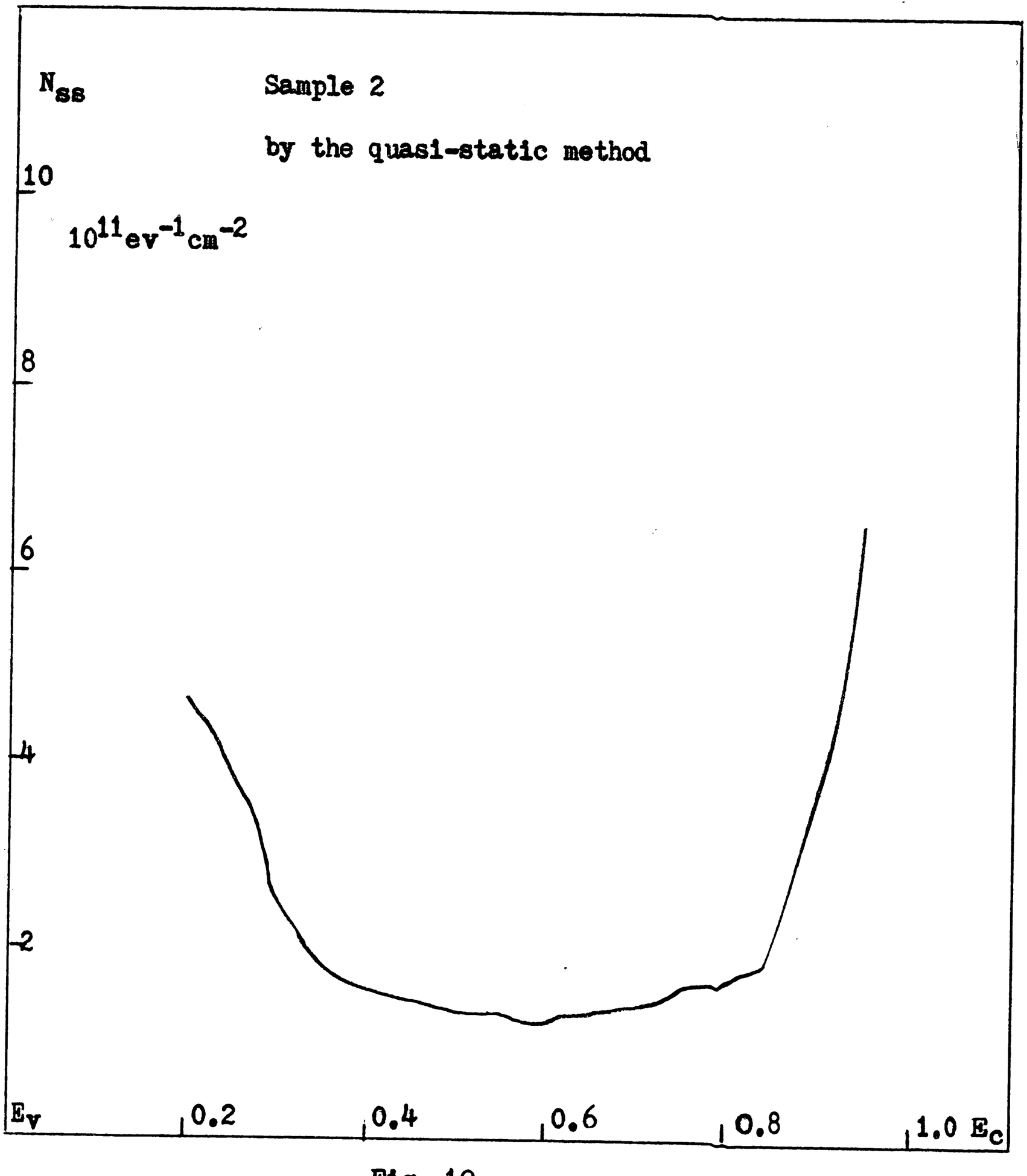

N_{ss}
Sample 2
by the quasi-static method
10
$10^{11} ev^{-1} cm^{-2}$
8
6
4
2
E_v
0.2
0.4
0.6
0.8
1.0 E_c

Fig. 19

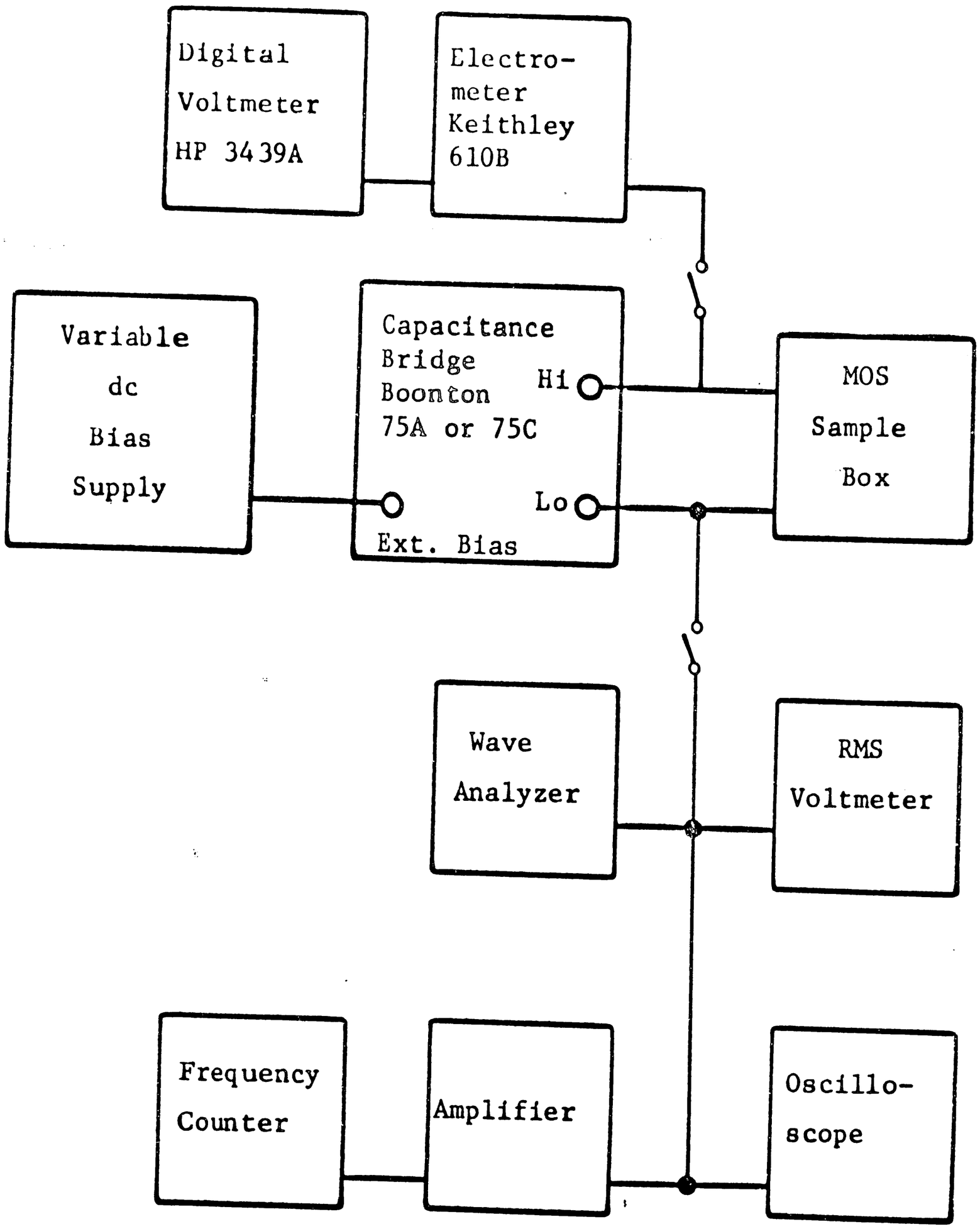

Digital
Voltmeter
HP 3439A
Electro-
meter
Keithley
610B
Variable
dc
Bias
Supply
Capacitance
Bridge
Boonton
75A or 75C
Hi
Lo
Ext. Bias
MOS
Sample
Box
Wave
Analyzer
RMS
Voltmeter
Frequency
Counter
Amplifier
Oscillo-
scope

Fig.20

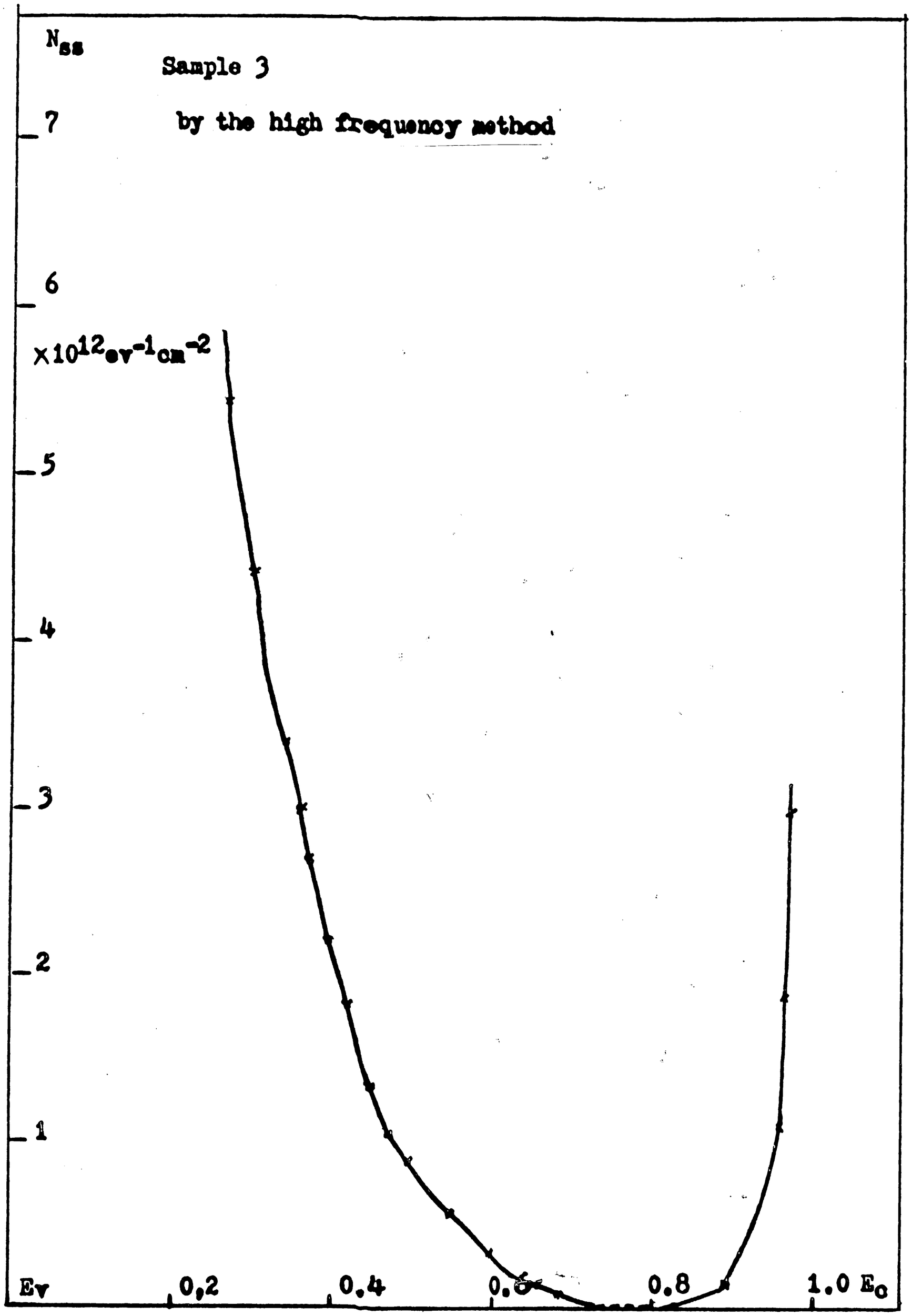

N_{ss}
Sample 3
by the high frequency method
7
6
$\times 10^{12} ev^{-1} cm^{-2}$
5
4
3
2
1
Ev
0,2
0.4
0.6
0.8
1.0 E_c

Fig. 21

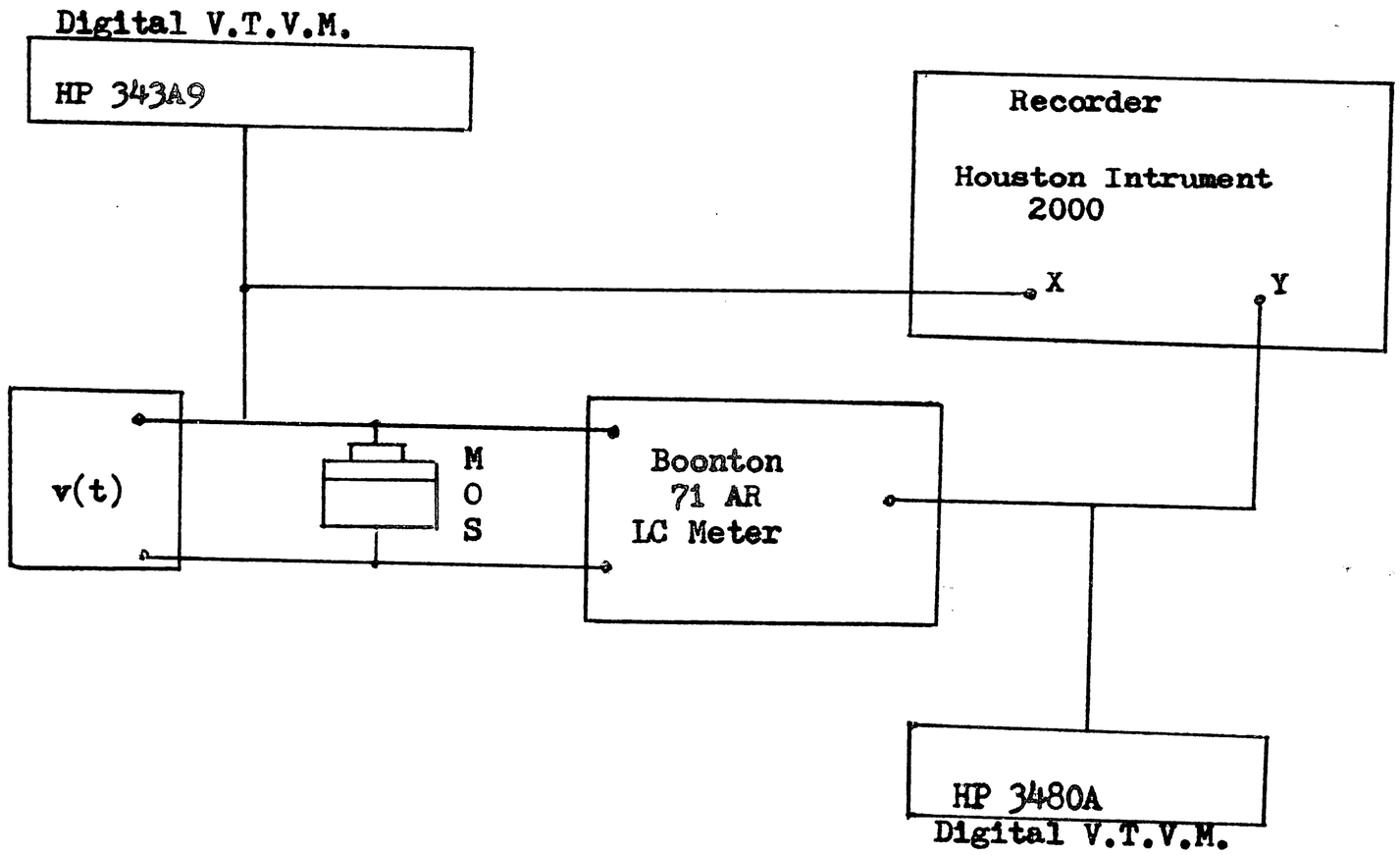

Digital V.T.V.M.
HP 343A9
Recorder
Houston Intrument
2000
X
Y
Ramping
Generator
v(t)
M
O
S
Boonton
71 AR
LC Meter
HP 3480A
Digital V.T.V.M.

Fig. 22

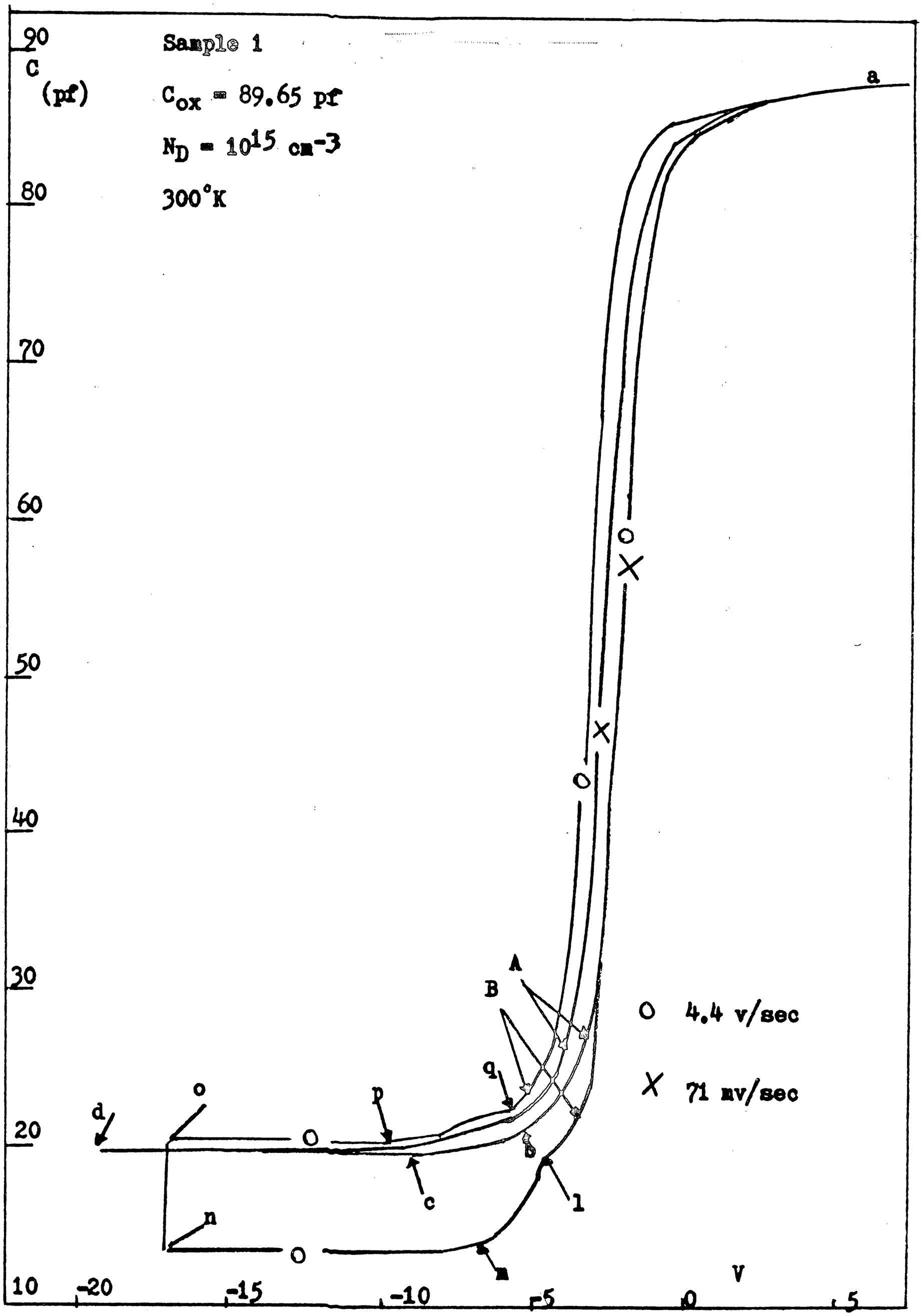
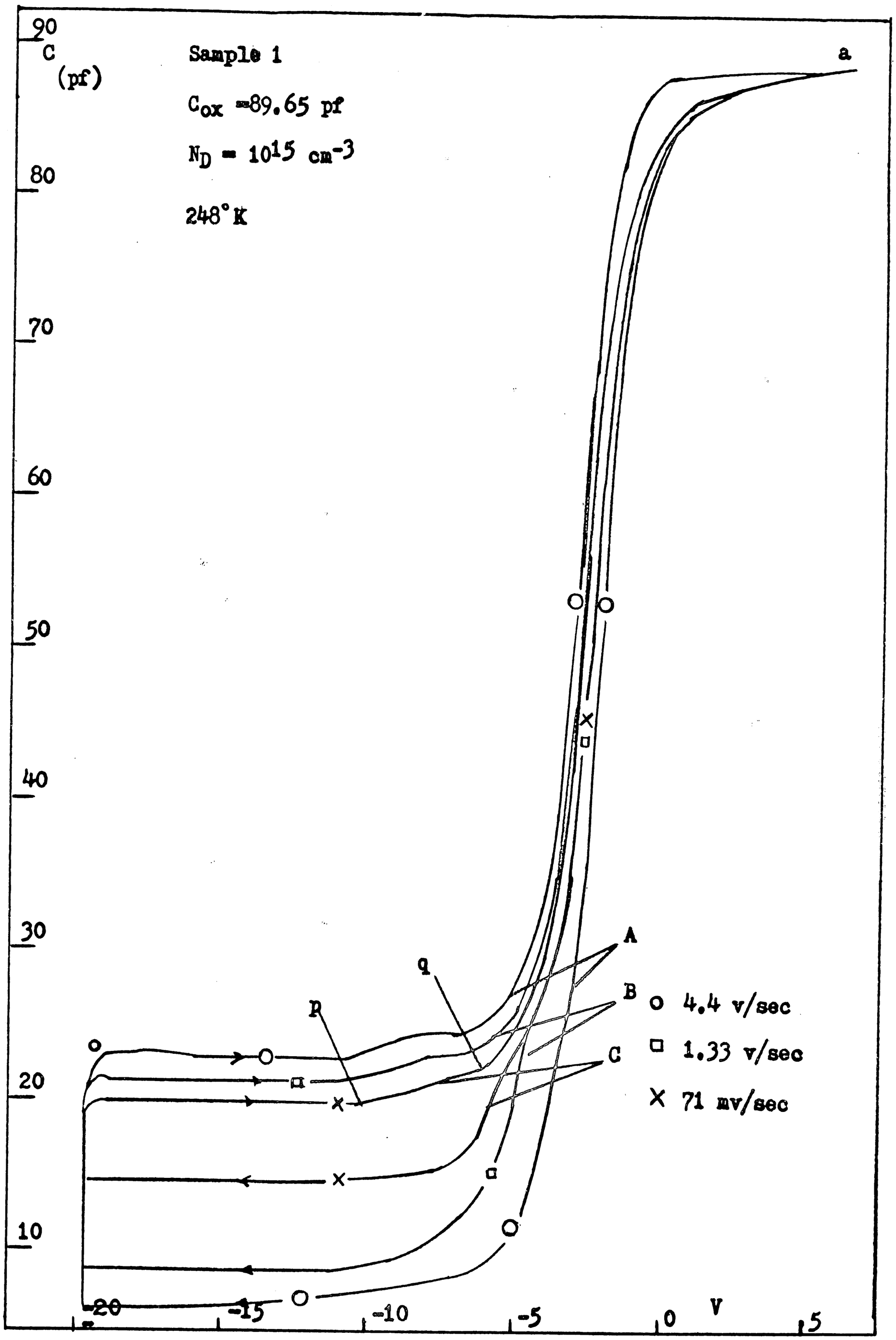

Sample 1
C_{ox} = 89.65 pf
$N_D = 10^{15}$ cm-3
300°K
C (pf)
90
80
70
60
50
40
30
20
10
-20
-15
-10
-5
0
5
V
a
o
x
o
x
A
B
q
p
o
d
o
o
b
c
l
n
o
■
O 4.4 v/sec
X 71 mv/sec

Fig. 23


C
(pf)
90
80
70
60
50
40
30
20
10
Sample 1
C_{ox} =89.65 pf
$N_D = 10^{15}$ cm^{-3}
248°K
a
A
B
C
P
q
o 4.4 v/sec
□ 1.33 v/sec
X 71 mv/sec
-20
-15
-10
-5
0
V
5

-67-

Fig. 24

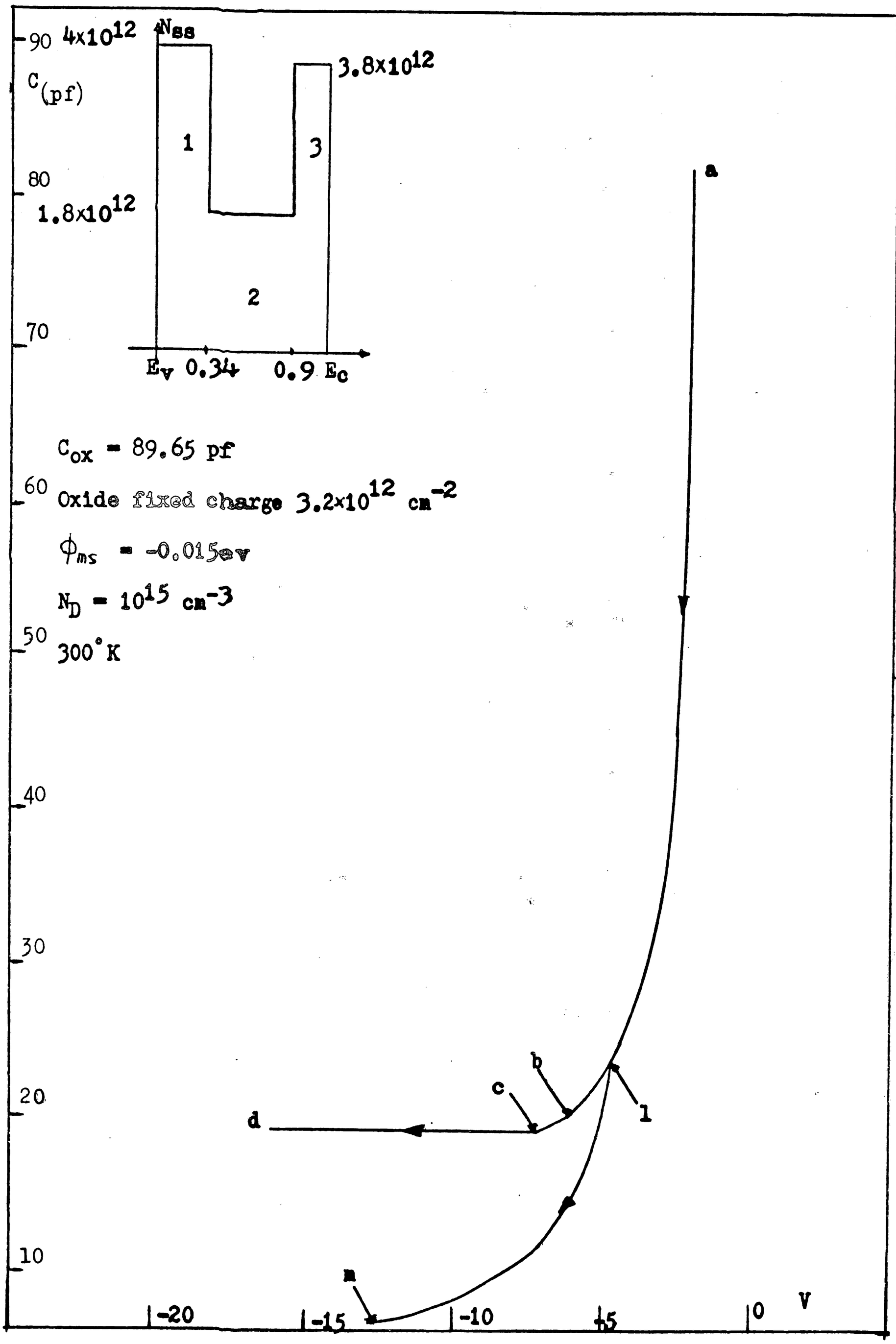

90
80
70
60
50
40
30
20
10
$C_{(pf)}$
4×10^{12} N_{ss}
3.8×10^{12}
1.8×10^{12}
1
2
3
E_v 0.34
0.9 E_c
C_{ox} = 89.65 pf
Oxide fixed charge 3.2×10^{12} cm^{-2}
ϕ_{ms} = -0.015ev
$N_D = 10^{15}$ cm^{-3}
300°K
a
b
c
d
1
-20
-15
-10
-5
0
V

Fig. 25

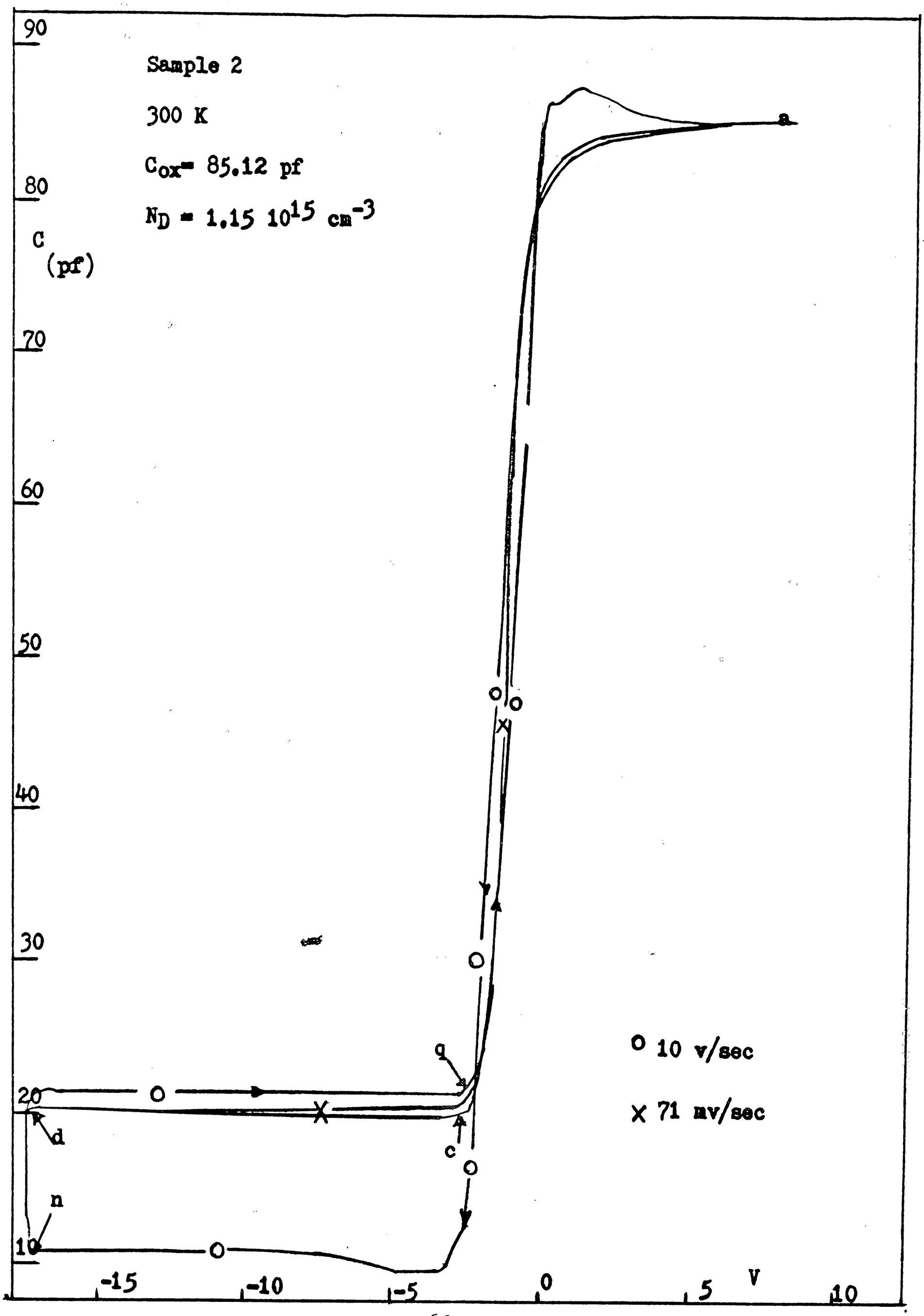

Sample 2
300 K
C_{ox}= 85.12 pf
N_D = 1.15 10^{15} cm^{-3}
C (pf)
90
80
70
60
50
40
30
20
10
-15
-10
-5
0
5
10
V
a
q
d
c
n
O 10 v/sec
X 71 mv/sec

Fig. 26

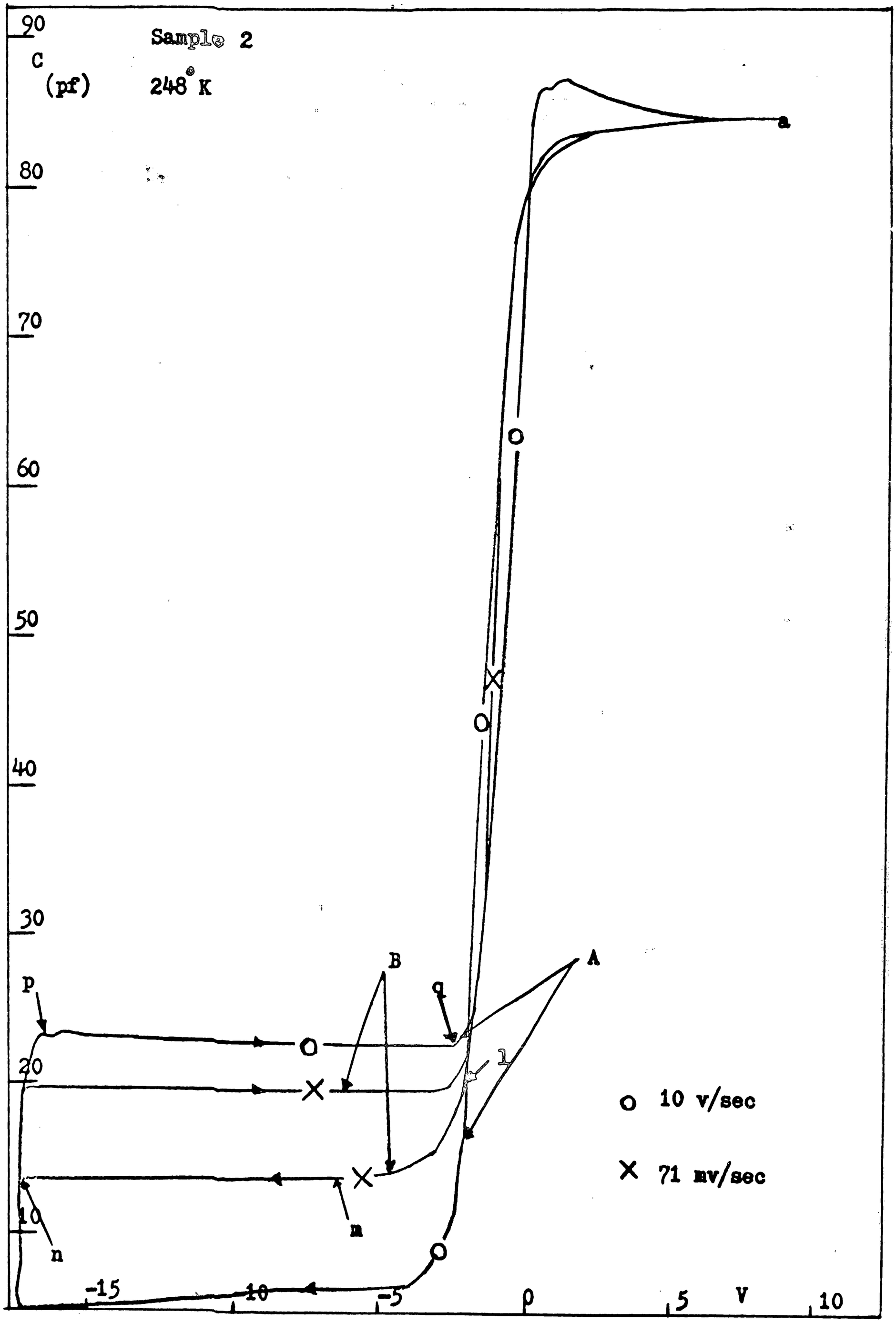

90
C
(pf)
Sample 2
248° K
80
70
60
50
40
30
20
10
a
O
X
O
B
A
P
q
1
n
m
-15
-10
-5
ρ
5
V
10
O 10 v/sec
X 71 mv/sec

Fig. 27

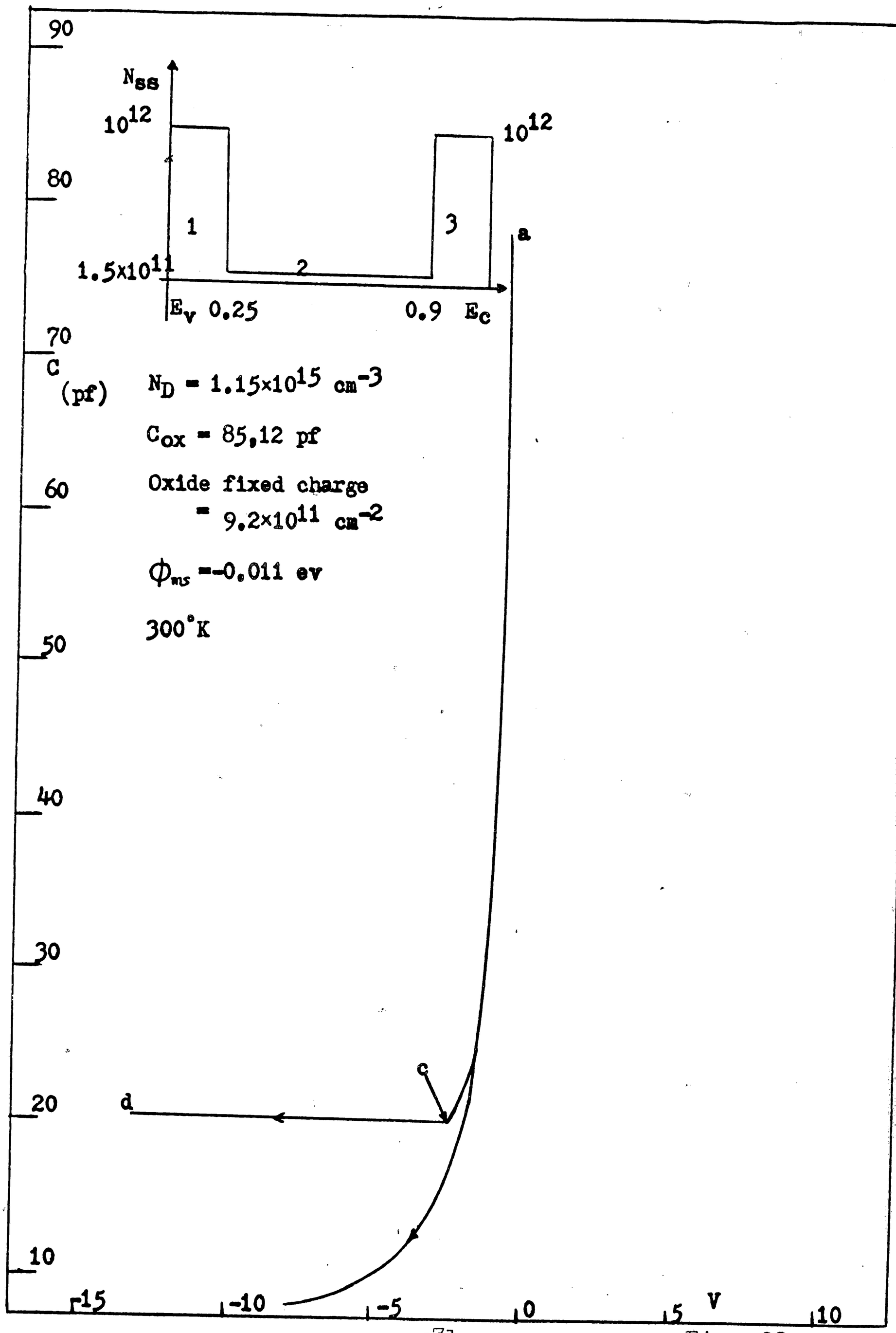

90
80
70
60
50
40
30
20
10
N_{ss}
10^{12}
10^{12}
1
2
3
a
1.5×10^{11}
E_v 0.25
0.9 E_c
C (pf)
$N_D = 1.15\times10^{15}$ cm^{-3}
C_{ox} = 85.12 pf
Oxide fixed charge
$= 9.2\times10^{11}$ cm^{-2}
ϕ_{ms} = -0.011 ev
300°K
c
d
-15
-10
-5
0
5
10
V

Fig. 28

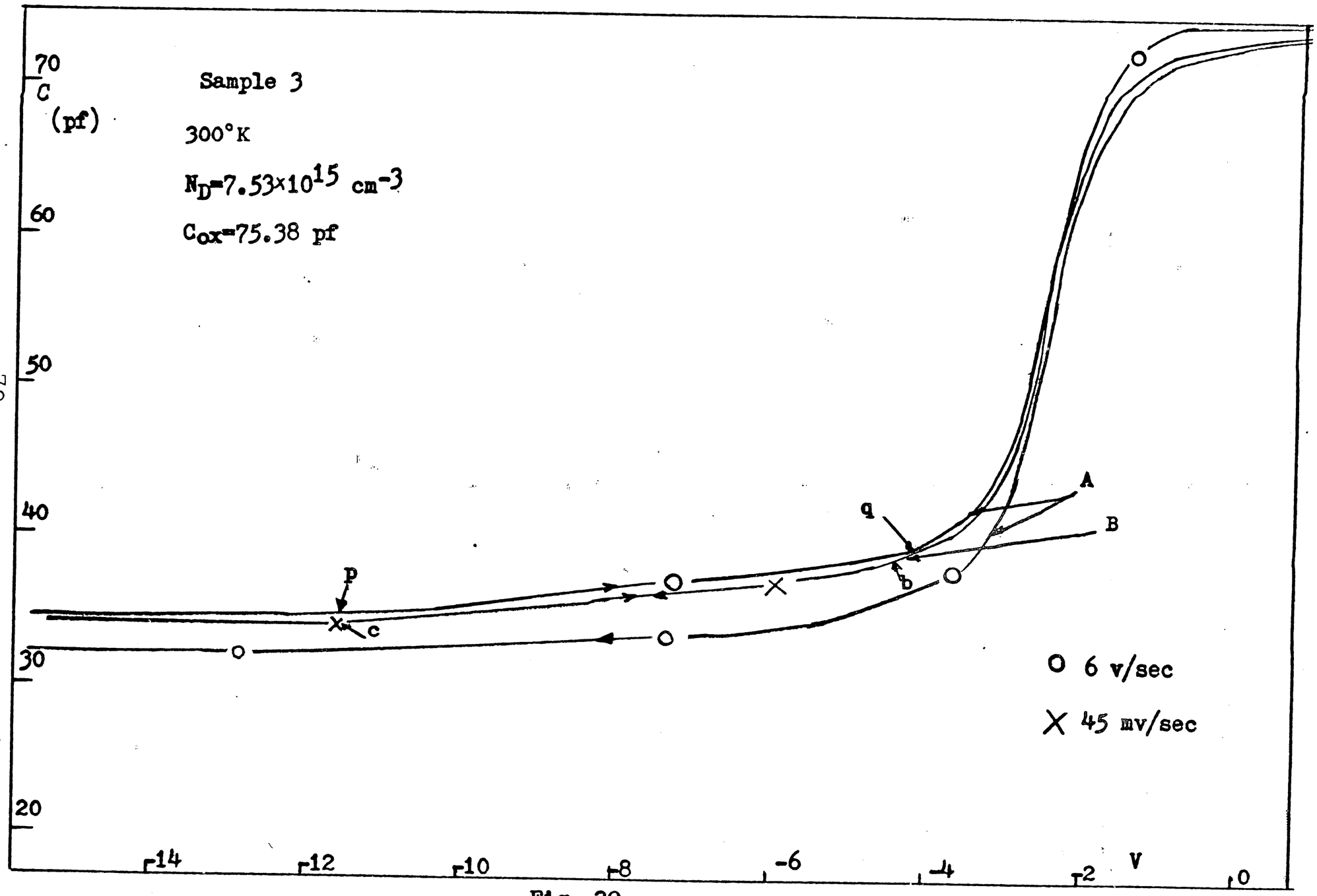

70
C
(pf)
60
50
40
30
20
Sample 3
300°K
$N_D=7.53\times10^{15}$ cm-3
$C_{ox}=75.38$ pf
O
A
B
q
p
c
b
O 6 v/sec
X 45 mv/sec
-14
-12
-10
-8
-6
-4
-2
0
V

Fig. 29

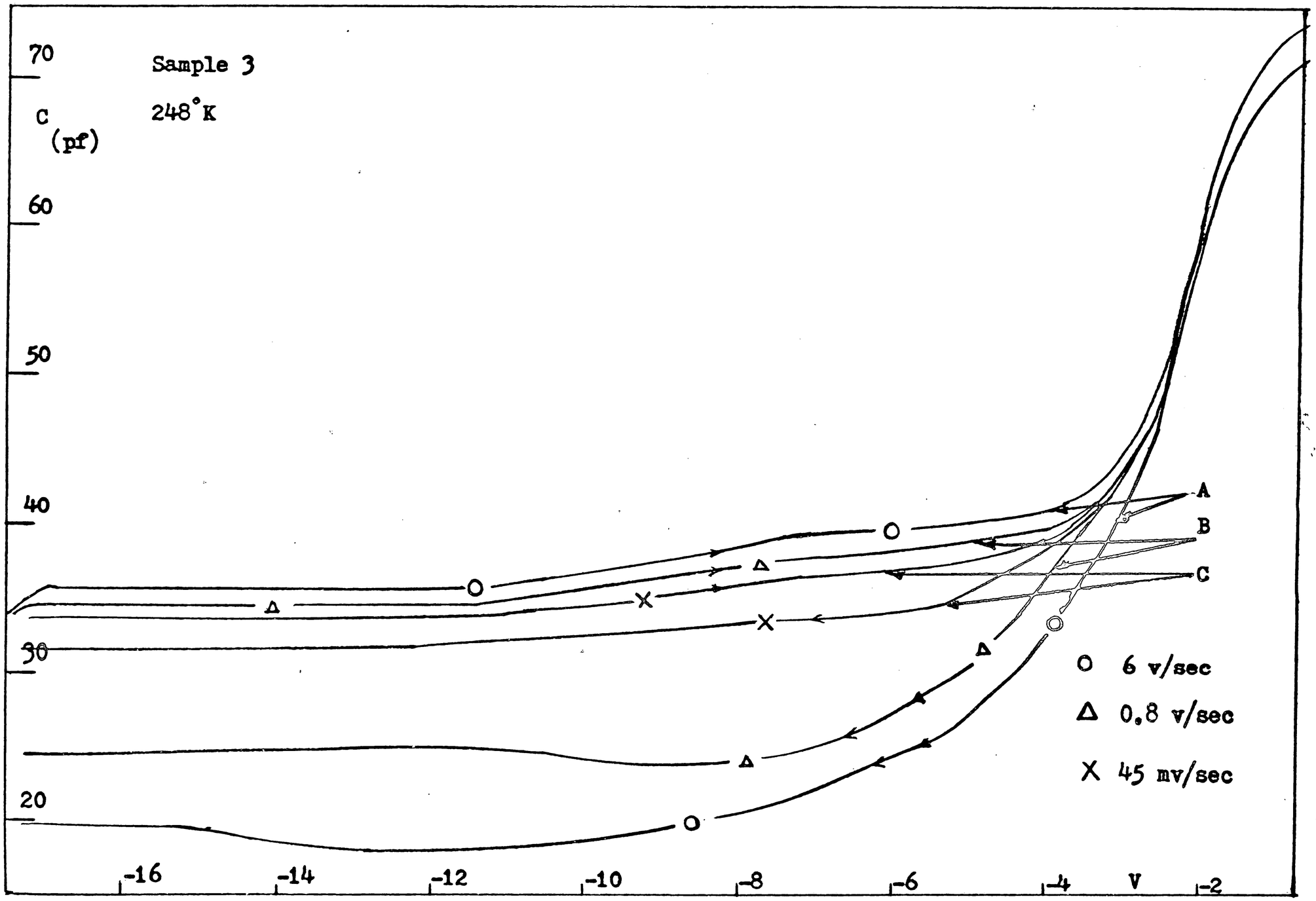

Sample 3
248°K
C (pf)
70
60
50
40
30
20
-16
-14
-12
-10
-8
-6
-4
V
-2
A
B
C
O 6 v/sec
Δ 0,8 v/sec
X 45 mv/sec

Fig. 30

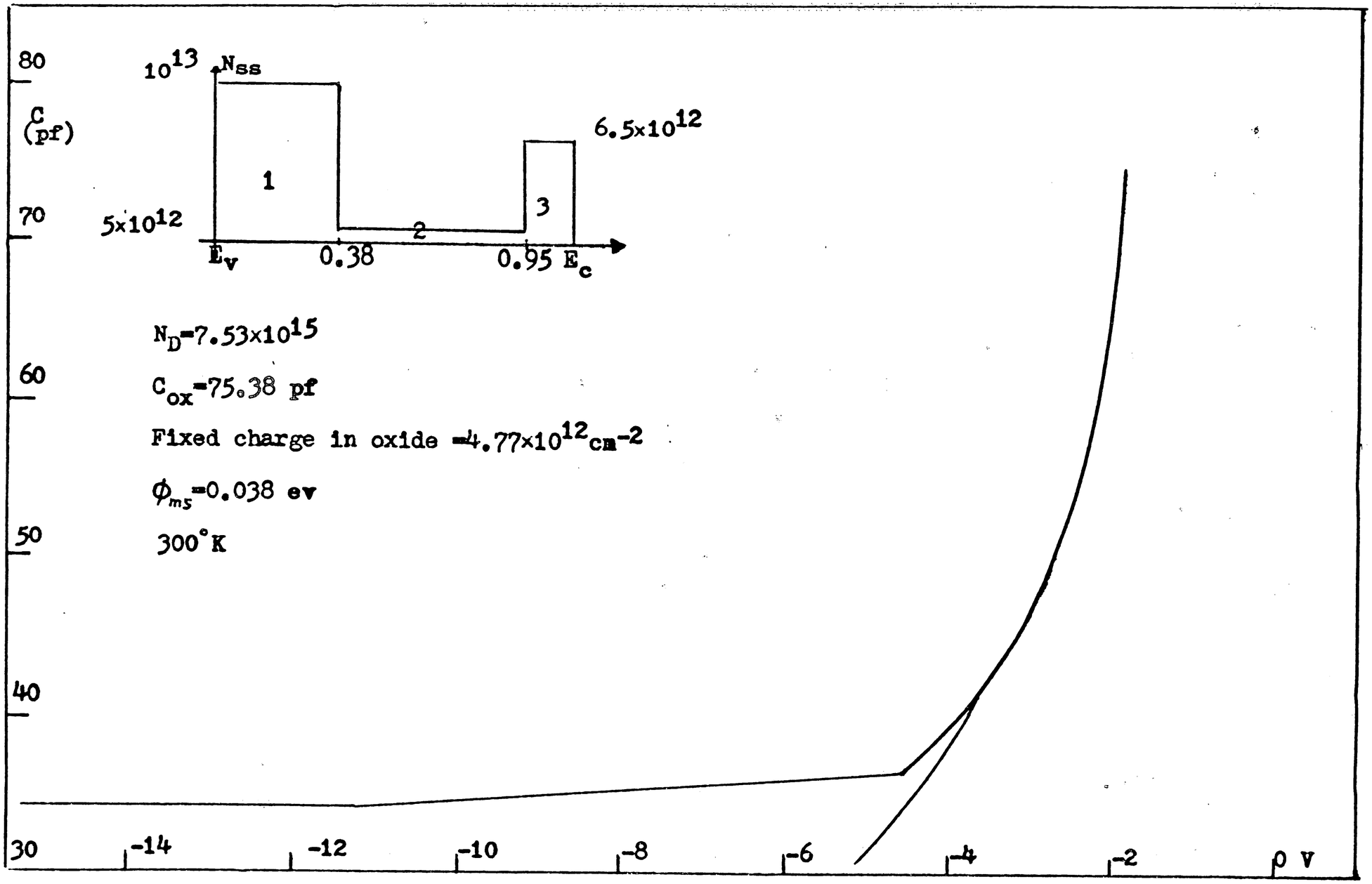

80
70
60
50
40
30
C (pf)
10^{13}
N_{ss}
6.5×10^{12}
5×10^{12}
1
2
3
E_v
0.38
0.95 E_c
$N_D=7.53\times10^{15}$
$C_{ox}=75.38$ pf
Fixed charge in oxide $=4.77\times10^{12}$ cm^{-2}
$\phi_{ms}=0.038$ ev
300°K
-14
-12
-10
-8
-6
-4
-2
0 V

Fig. 31

VITA

Chin-Che Wang was born on September 12, 1947 in Chia-Yi, Taiwan to Dah-Shou and Lai-Hau Wang. He received a Bachelor of Science degree in Electrical Engineering from Cheng Kung University, Tainan, Taiwan in June 1969. After one year military service, he had served as a teaching assistant in National Chiao-Tung University, Hsin-Chu, Taiwan from Aug. 1970 to July 1971. At the same time, he enrolled as a graduate student of the Institute of Management Science, Chiao-Tung University. In Aug. 1971, he came to Lehigh University, Bethlehem, Pennsylvania. He is currently working toward the M. S. degree in electrical engineering under Professor W. E. Dahlke. While at Lehigh University, he has held Teaching Assistantship and Research Assistantship.